

AM64x/AM243x GENERAL PURPOSE EVM BOARD
PROC101C

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REV	C
VER	1.1



REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	16th AUG 2022	Symbol Updated to Match Datasheet Pin Names	Mistral Design Team	AJIT MB	AJIT MB

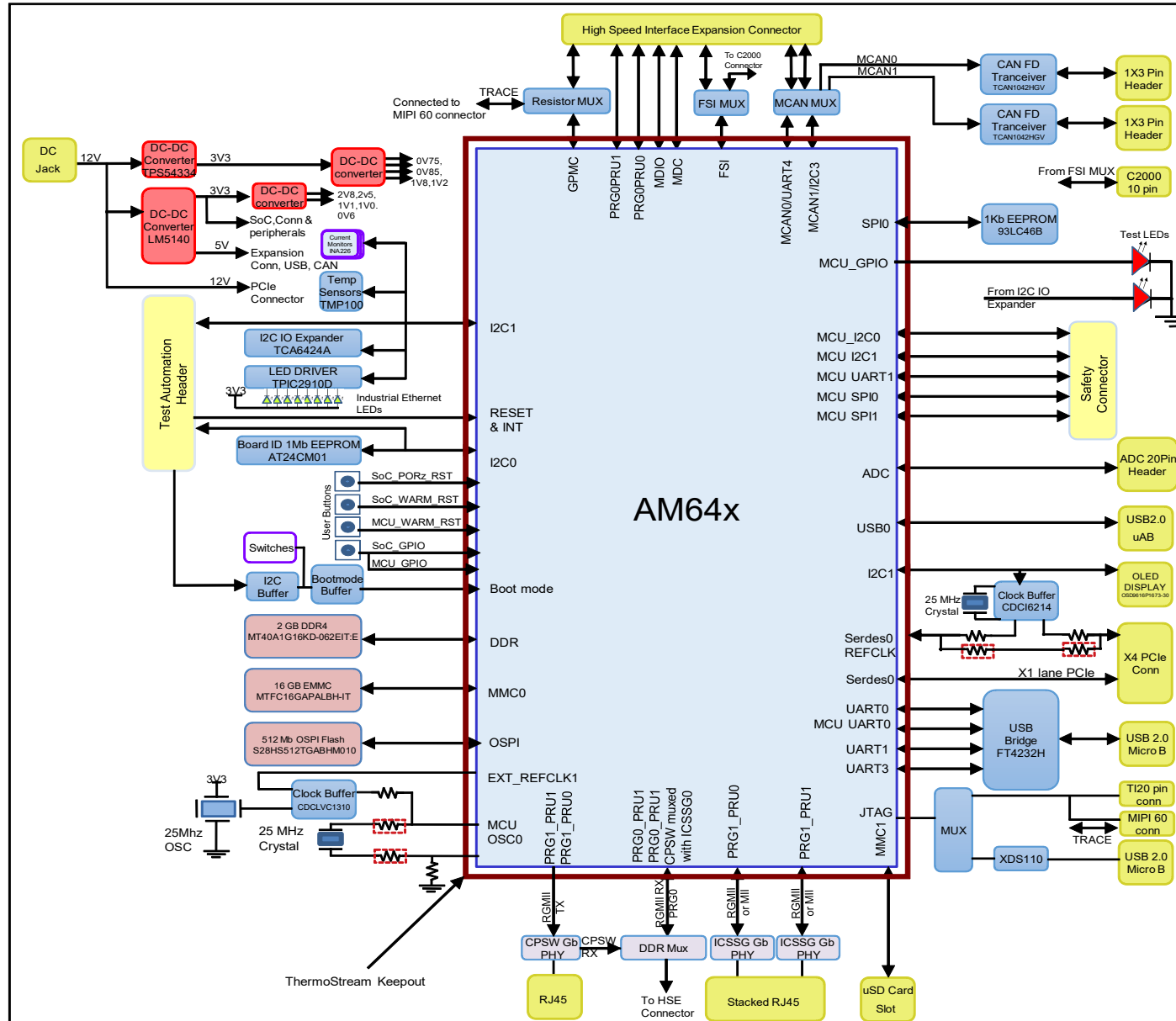
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Title REVISION HISTORY

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
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BLOCK DIAGRAM_AM64x_EVM



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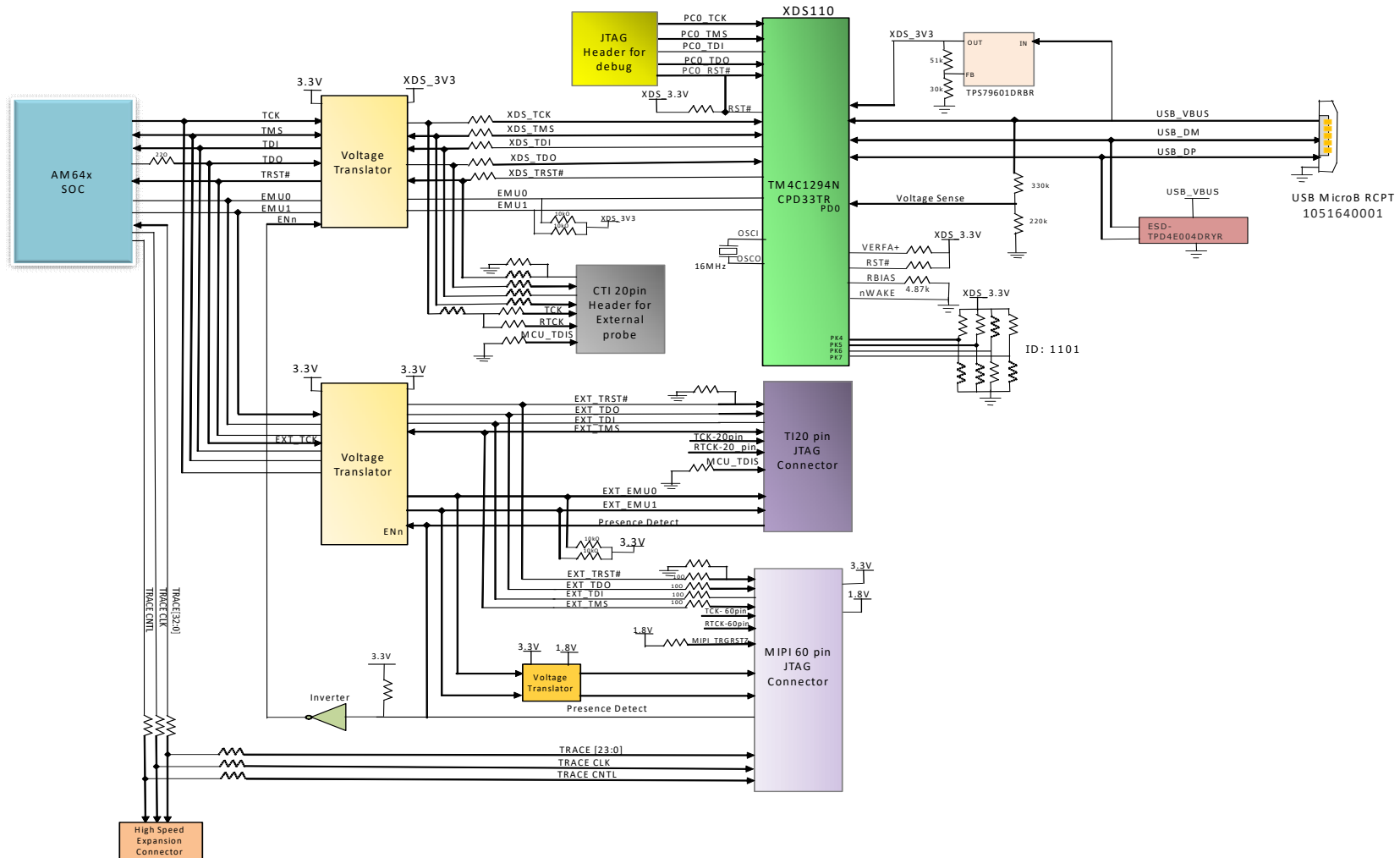
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Size	
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C	Variant Name = PROC101C(003) TMDS64HSEVM	E
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BLOCK DIAGRAM_XDS110



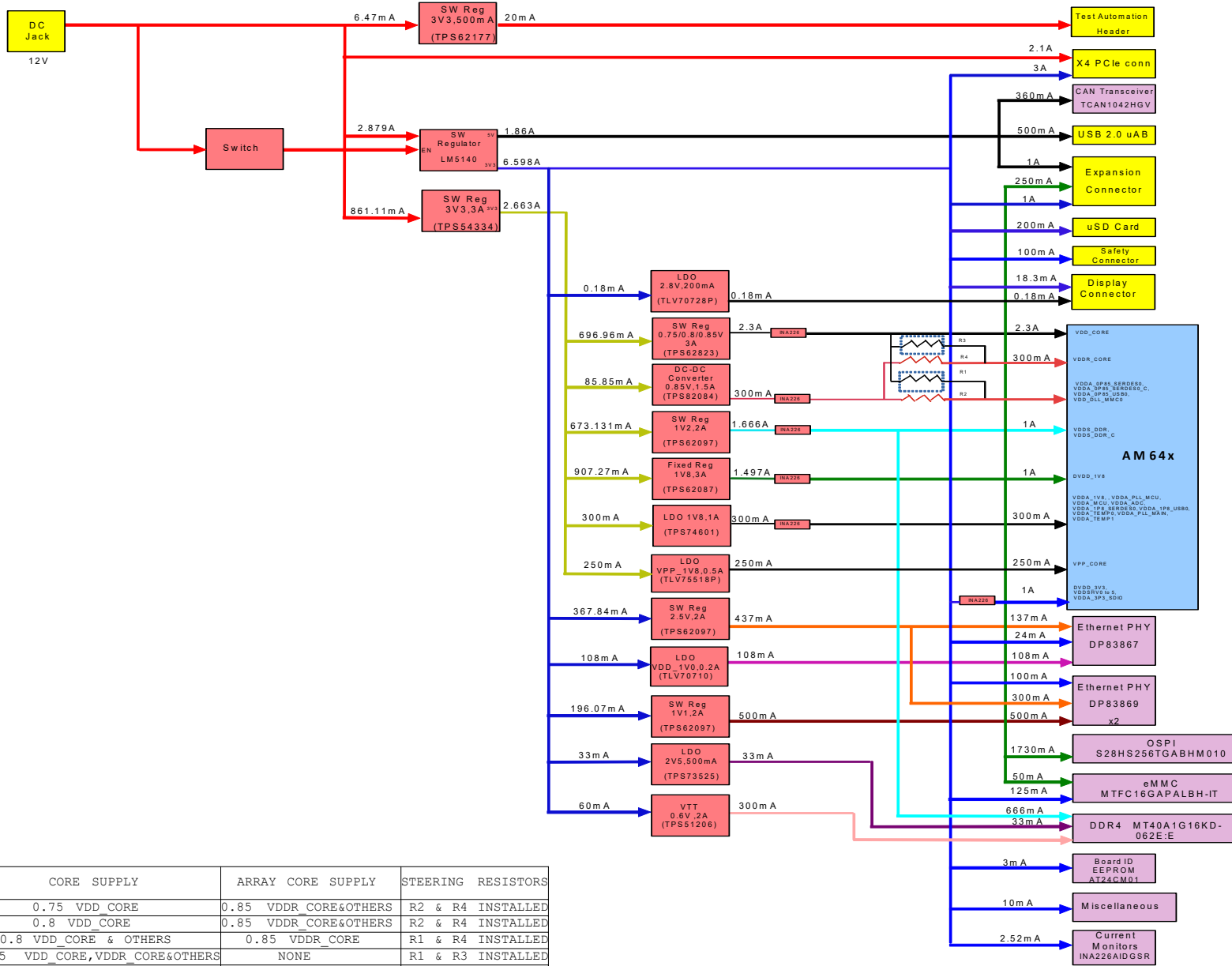
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Title BLOCK DIAGRAM_XDS110

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
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POWER FLOW DIAGRAM



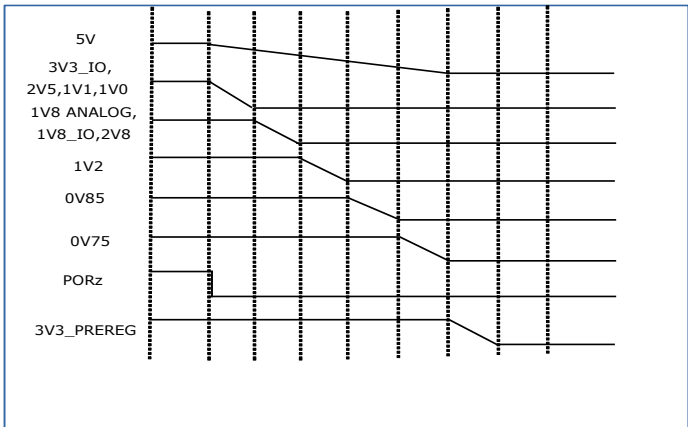
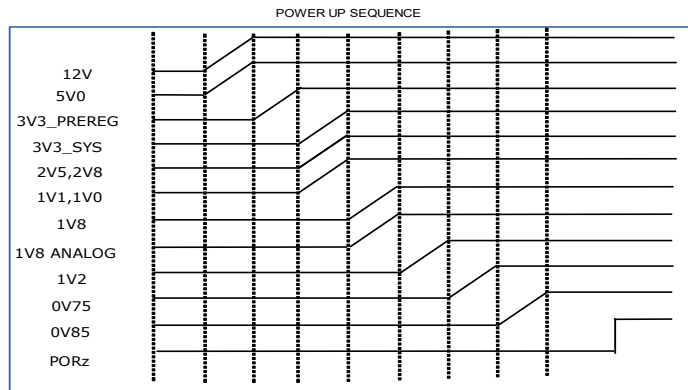
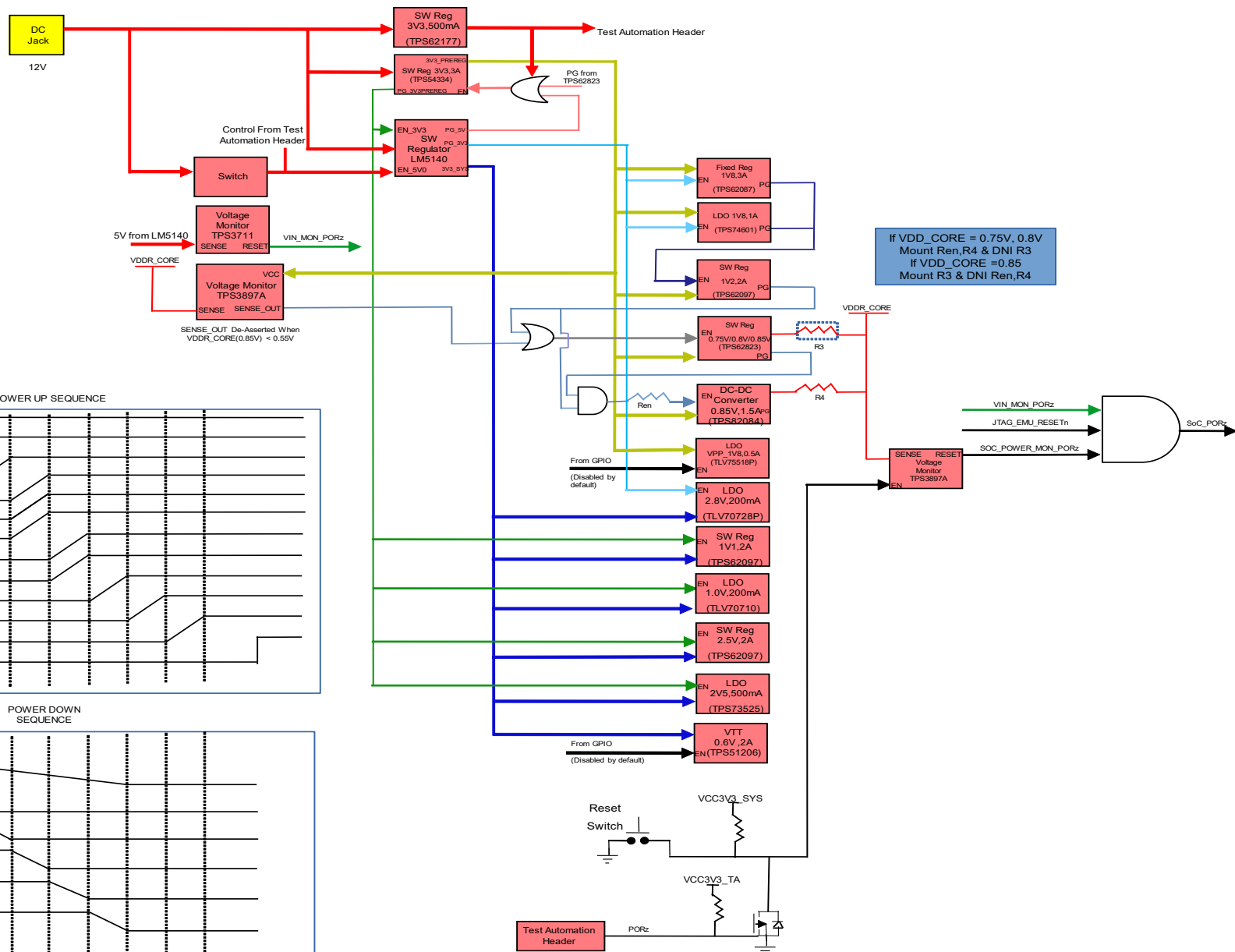
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Title POWER FLOW DIAGRAM

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
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POWER SEQUENCE



GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETh	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

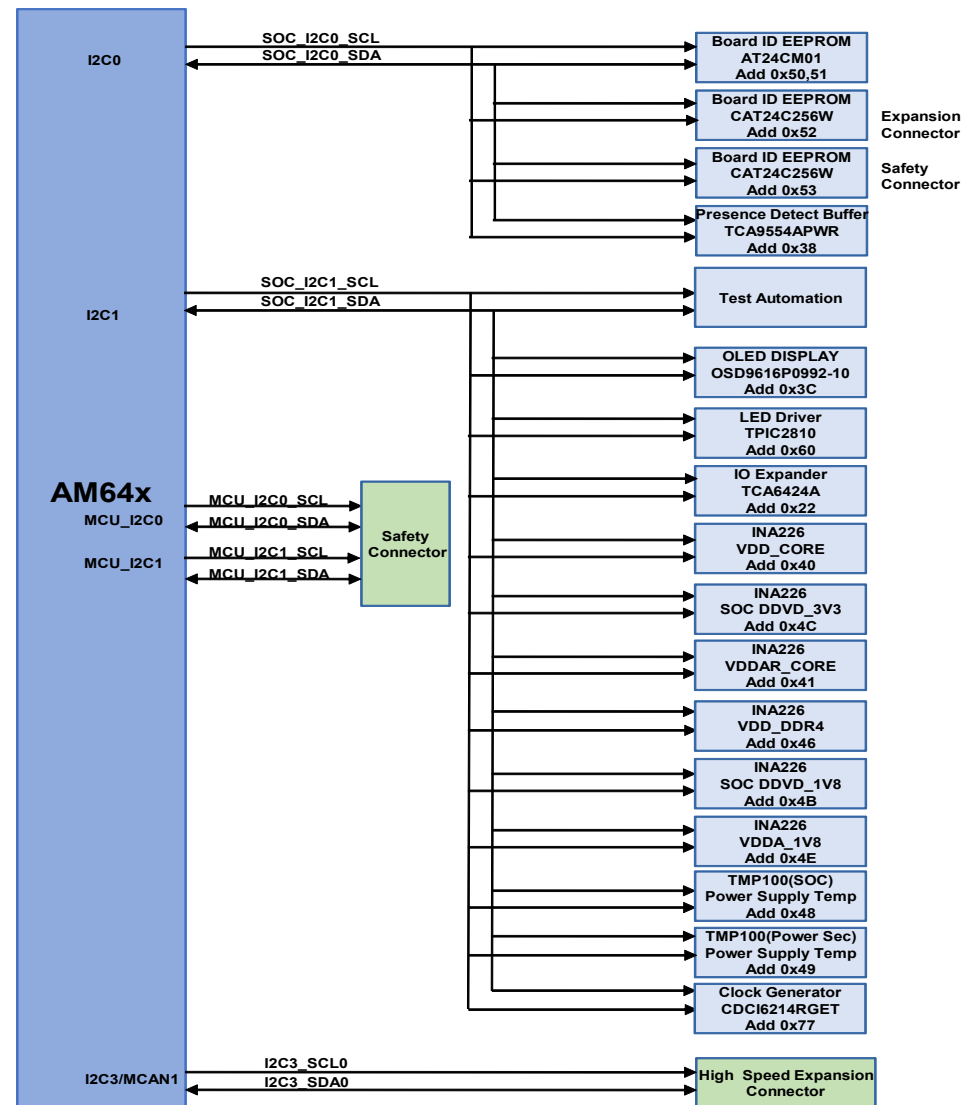
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
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I2C TREE



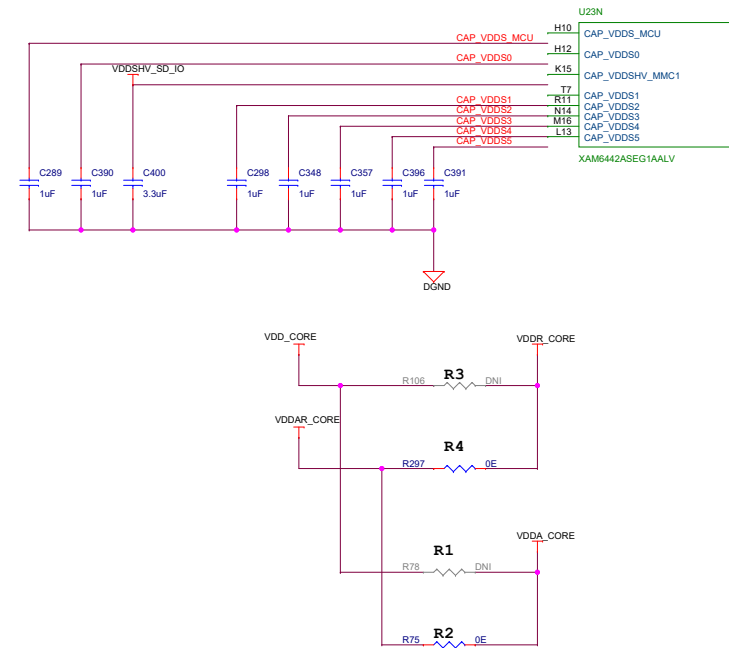
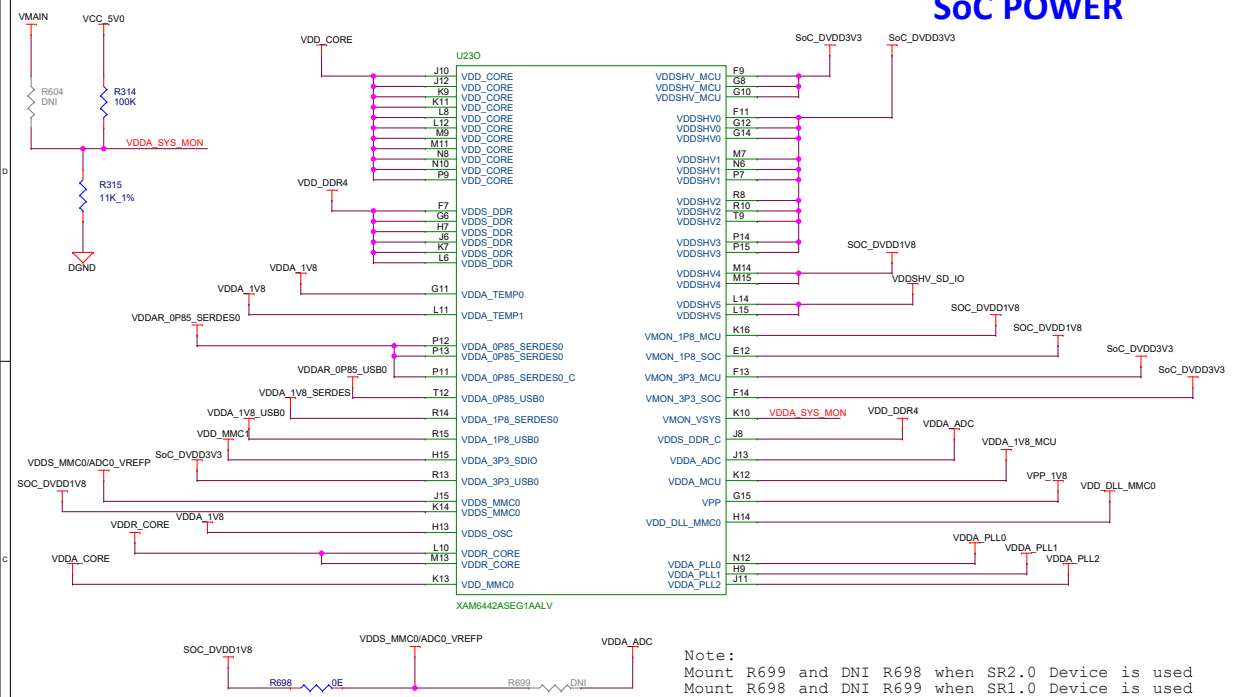
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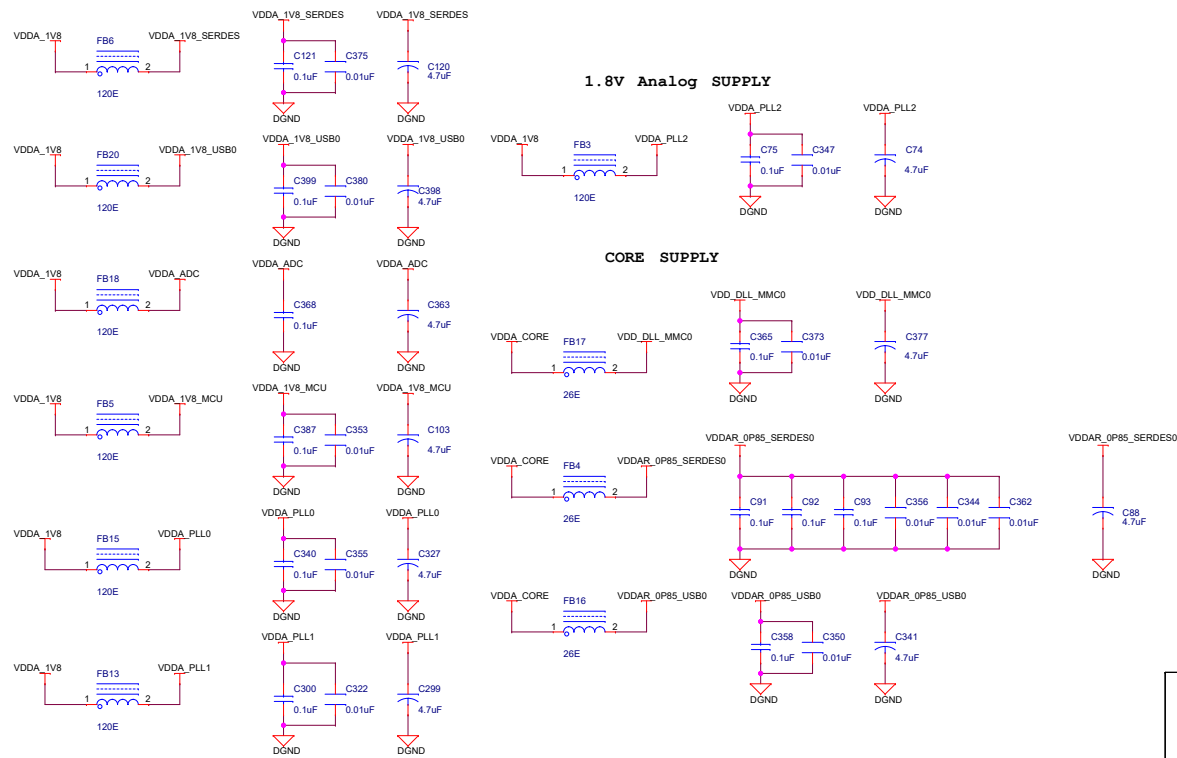
Title I2C TREE

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
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SoC POWER



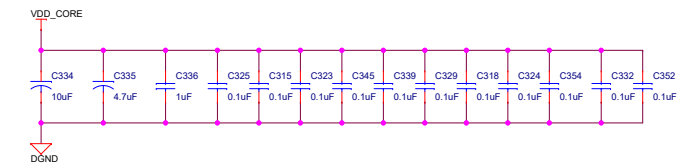
1.8V Analog SUPPLY



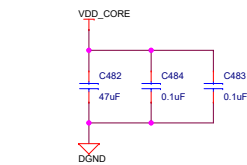
CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED



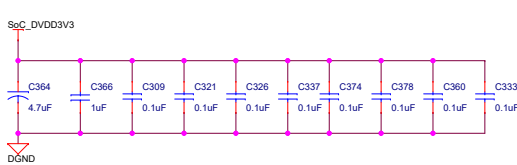
SoC POWER Decaps



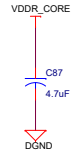
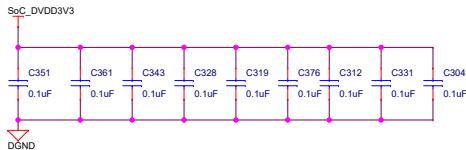
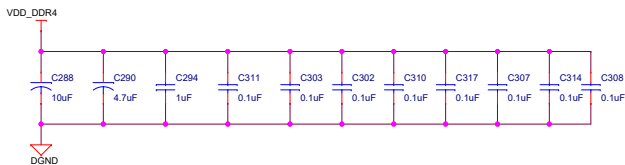
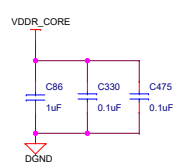
Place one 0.1uF cap near each Pin



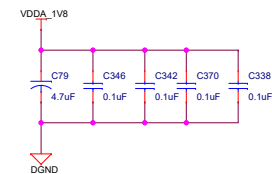
To place after current sense resitor on VDD_CORE plane



Place one 0.1uF cap near each Pin

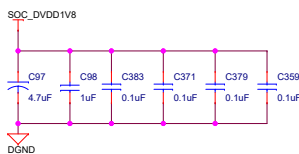
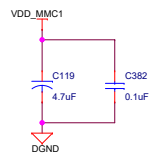


VDD ARRAY CORE

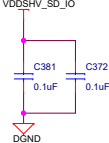


Place one 0.1uF cap near each Pin

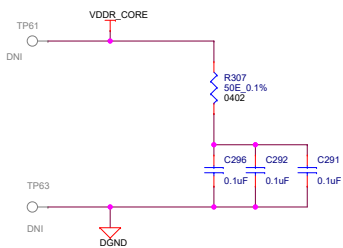
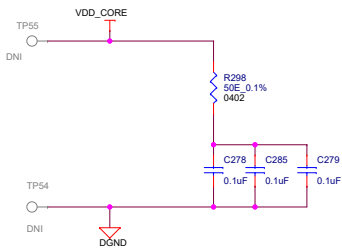
VDDA_3P3_SDIO



Place one 0.1uF cap near each Pin



Core & Array Core Supply Kelvin Sensing



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Title SOC POWER CAPS

Size Variant Name = PROC101C(003) TMD564HSEVM

Date: Monday, August 22, 2022

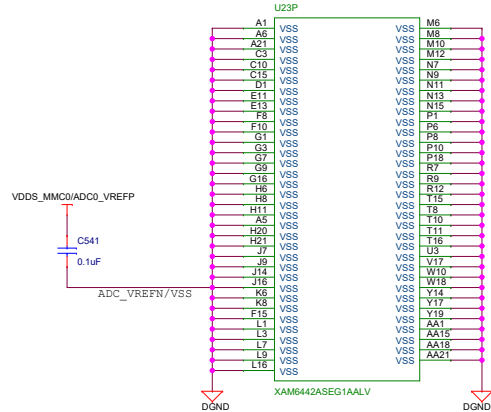
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Rev

E2

SoC POWER - VSS

CAD Note:
Place CAP C541
between pins
J15 and J16



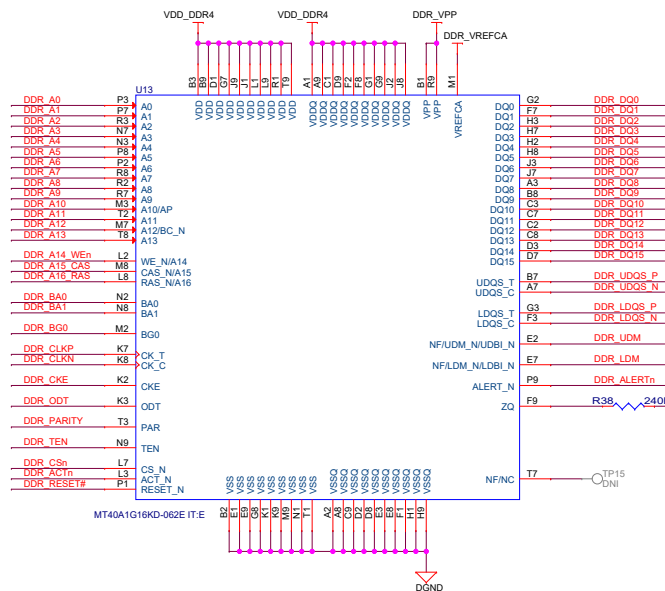
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Title SOC VSS

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
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U23G				
D2	DDR_D0	DDR0_D00	B2	DDR_LDM
D5	DDR_D1	DDR0_DM0	B2	DDR_UDM
E2	DDR_A1	DDR0_DM1		
D3	DDR_A2		A3	DDR_D00
D3	DDR_A3	DDR0_D00	A2	DDR_D05
F2	DDR_A4	DDR0_D01	B5	DDR_D04
F2	DDR_A5	DDR0_D02	A4	DDR_D01
L5	DDR_A6	DDR0_D03	B3	DDR_D03
A7	DDR_A7	DDR0_D04	C2	DDR_D06
J4	DDR_A8	DDR0_D05	C4	DDR_D07
K3	DDR_A9	DDR0_D06	B4	DDR_D02
J1	DDR_A10	DDR0_D07	N5	DDR_D08
D7	DDR_A11	DDR0_D08	L4	DDR_D015
K4	DDR_A12	DDR0_D09	L2	DDR_D014
	DDR_A13	DDR0_D010	M5	DDR_D010
G4		DDR0_D011	N4	DDR_D09
G5	DDR_BA0	DDR0_D012	N3	DDR_D012
	DDR_BA1	DDR0_D013	M4	DDR_D011
G2		DDR0_D014	N2	DDR_D013
H3	DDR_B00	DDR0_D015		
	DDR_B01		C1	DDR_LDQS_P
		DDR0_D050		DDR_LDQS_N
E1	DDR_CK0	DDR0_D050_N		
	DDR_CK0_N		N1	DDR_UDQS_P
F4	DDR_CK00	DDR0_D051	M1	DDR_UDQS_N
F3	DDR_CKE1	DDR0_D051_N		
E3	DDR_CS0_N			
E4	DDR_CS1_N			
E5	DDR_ODT0			
F5	DDR_ODT1			
H2	DDR_ACT_N			
H1	DDR_ALERT_N			
H5	DDR_CAL0			
J5	DDR_CAS_N			
K5	DDR_PAR			
F6	DDR_RAS_N			
D5	DDR_RESETO_N			
H4	DDR_WE_N			



TERMINATION

The diagram illustrates the termination network for DDR4 signals. It shows two main termination points: VDD_DDR4 and VDDR_VTT. The VDD_DDR4 network includes resistors R69 (10K), R63 (DNI), R62 (1K_1%), and R64 (DNI). The VDDR_VTT network includes resistors R247 (DNI) and R258 (DNI). The diagram also shows the connection of DDR4 signals to the termination network, including DDR_CLKP, DDR_CLKN, DDR_B0, DDR_CKE, DDR_CSn, DDR_BA0, DDR_BA1, DDR_PARITY, DDR_A0, DDR_A1, DDR_A2, DDR_A3, DDR_A4, DDR_A7, DDR_A8, DDR_A9, DDR_A10, DDR_A11, DDR_A12, DDR_A13, DDR_A14, DDR_A15, DDR_A16, DDR_ACTn, and DDR_QDT. The termination network is connected to VDD_DDR4 and VDDR_VTT, and the signals are connected to the termination network through resistors R261, R267, R269, R46, R256, R273, R288, R85, R289, R90, R86, R89, R90, R287, R275, R77, R84, R91, R291, R83, R88, R71, R264, R271, R274, R87, and R258.

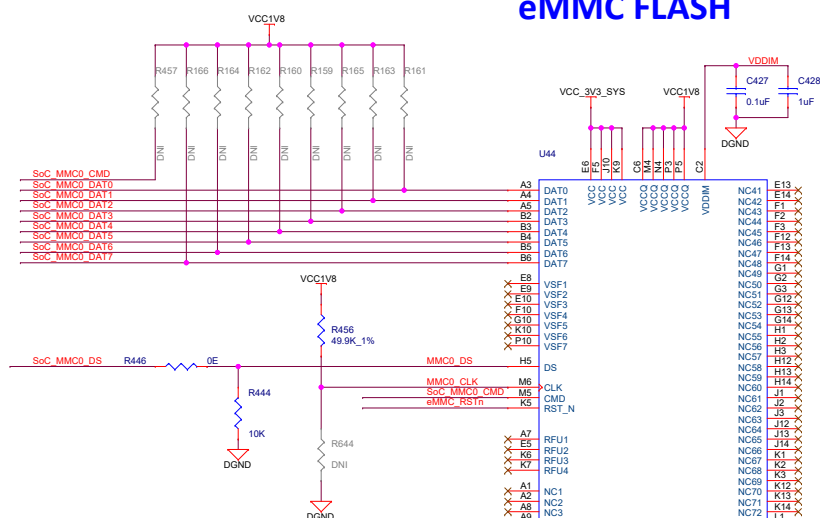
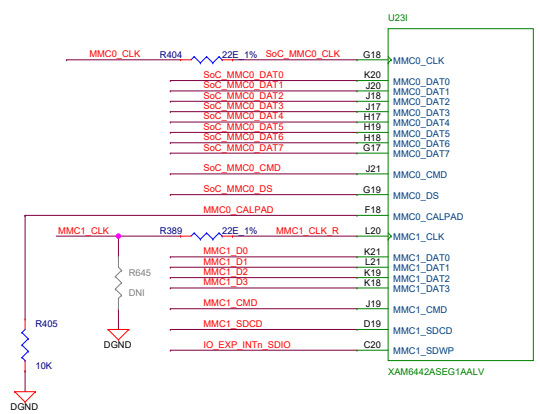


TEXAS
INSTRUMENTS

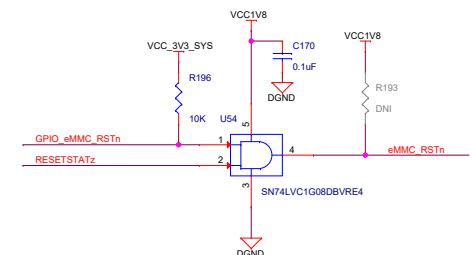
Size	Variant Name = PROC101C(003) TMD564HSEVM	
C		
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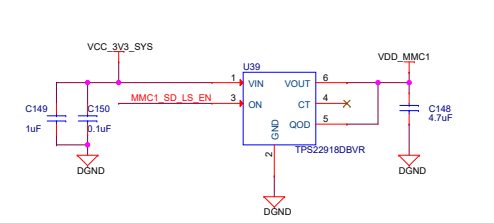
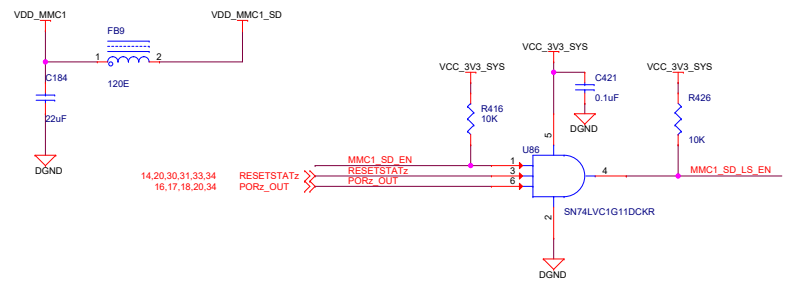
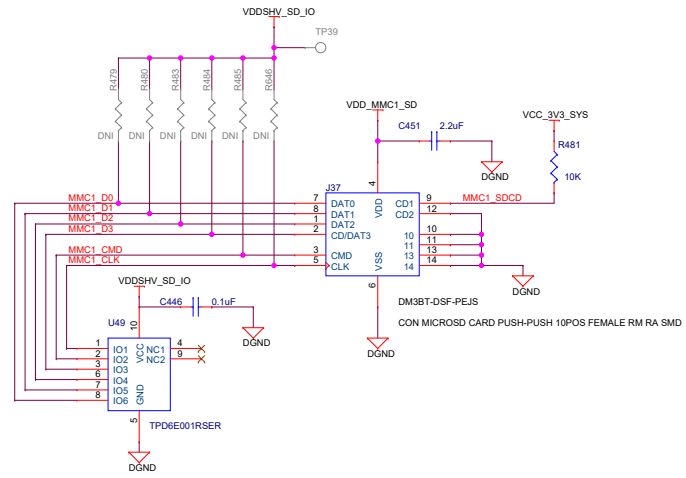
eMMC FLASH



eMMC FLASH RESET



SD CARD INTERFACE



Off Page Connections

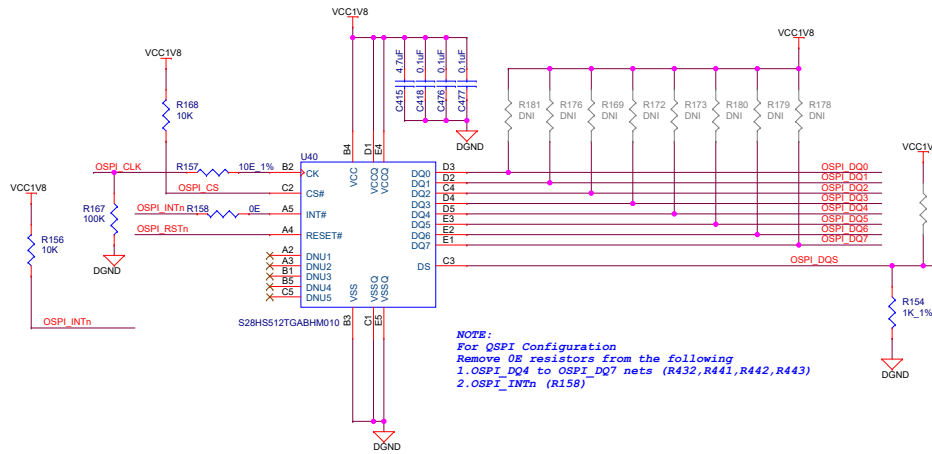
From 4	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

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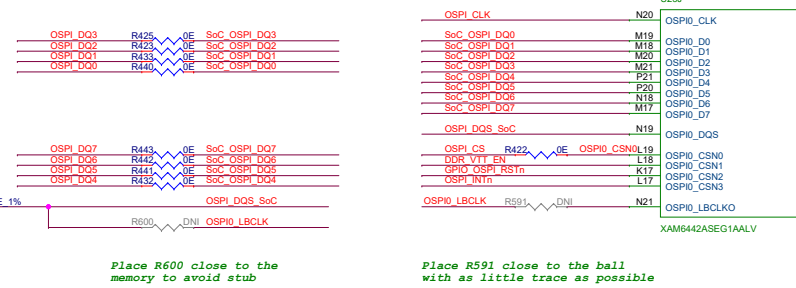


Title eMMC FLASH_SDCARD INTERFACE			
Size	Variant Name = PROC101C(003) TMD564HSEVM		Rev E2
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OSPI FLASH

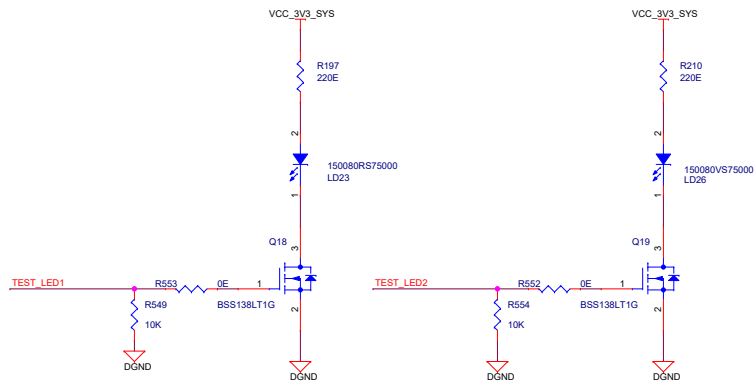


SOC OSPI INTERFACE

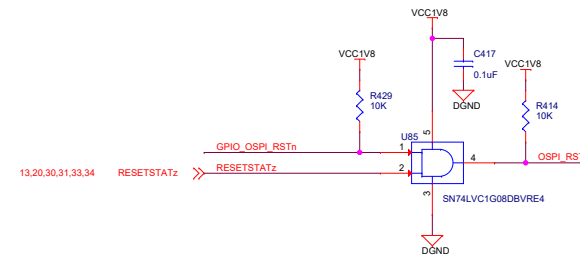


To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

USER TEST LED



OSPI FLASH RESET



Off Page Connections

TEST_LED1	TEST_LED1	33
TEST_LED2	TEST_LED2	34
DDR_VTT_EN	DDR_VTT_EN	33

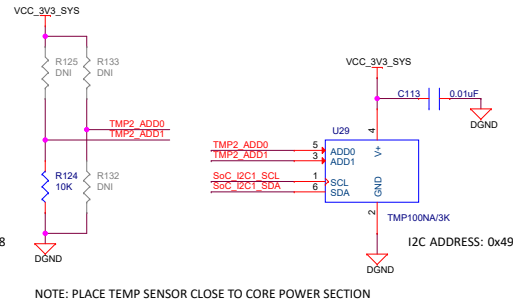
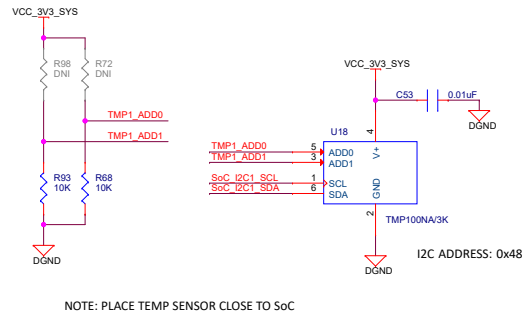
To Level Translator

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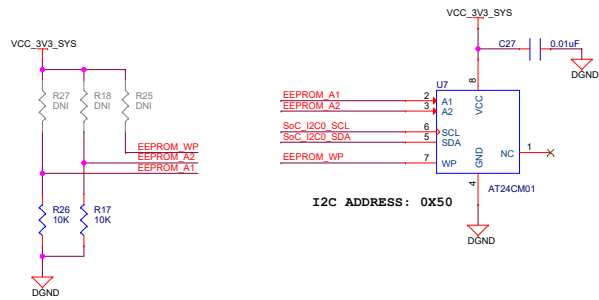
Title				OSPI			
Size		Variant Name = PROC101C(003) TMD564HSEVM				Rev	
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TEMPERATURE SENSOR

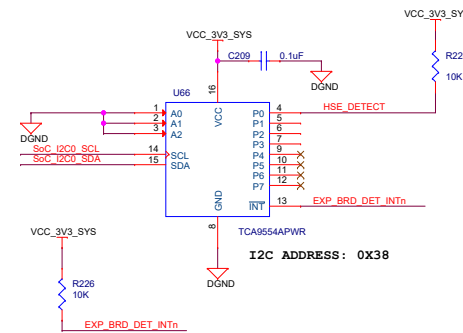


SoC I2C1 SCL DNI TP25
SoC I2C1 SDA DNI TP27

BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

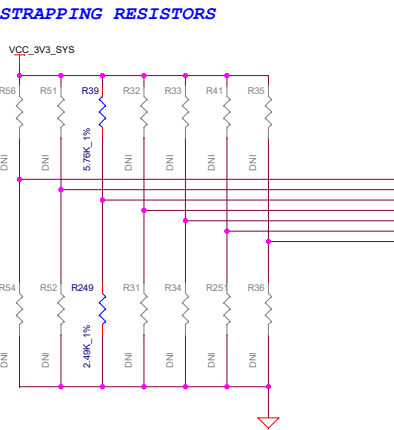
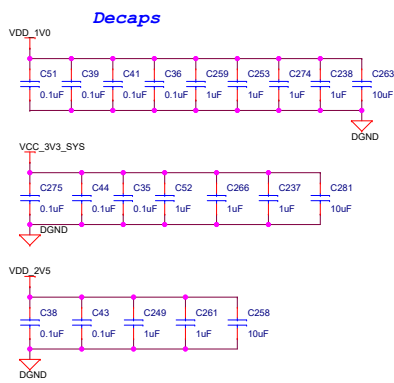
HSE_DETECT	←	HSE_DETECT	27
SoC I2C1 SDA	↔	SoC I2C1 SDA	19,21,29,30,31,32,33
SoC I2C1 SCL	↔	SoC I2C1 SCL	19,21,29,30,31,32,33
SoC I2C0 SDA	↔	SoC I2C0 SDA	27,29,33
SoC I2C0 SCL	↔	SoC I2C0 SCL	27,29,33

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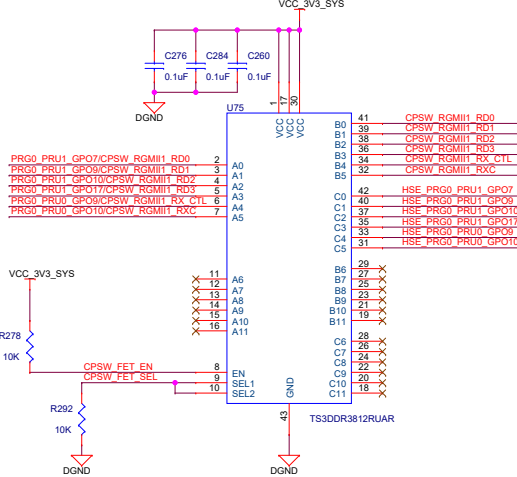
Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 15 of 40



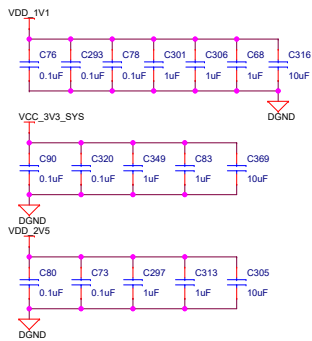
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns

CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS

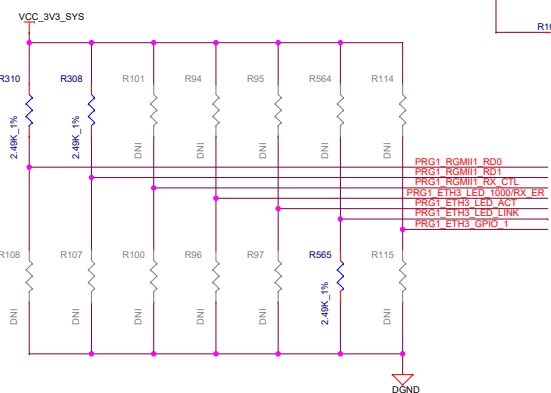


Size	Variant Name = PROC101C(003) TMD564HSEVM	
C		
Date:	Monday, August 22, 2022	Sheet 17 of 40

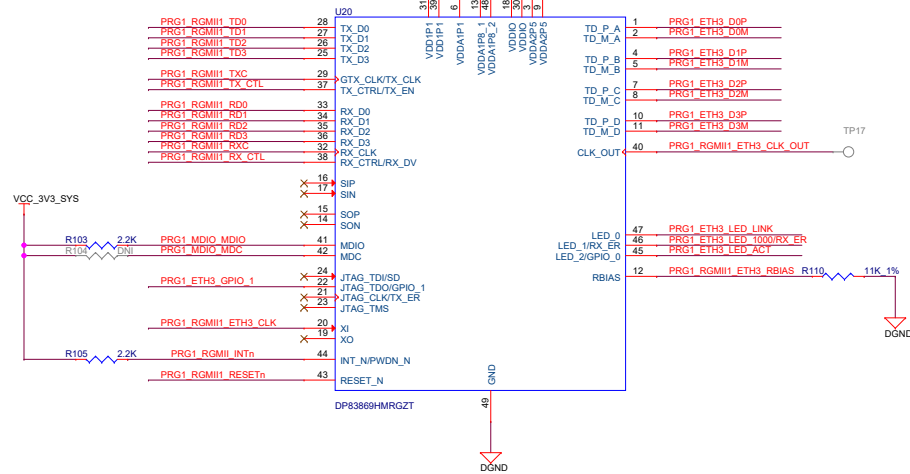
Decaps



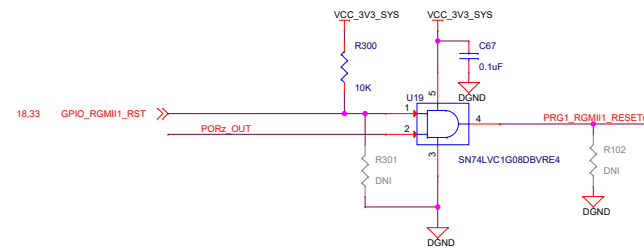
STRAPPING RESISTORS



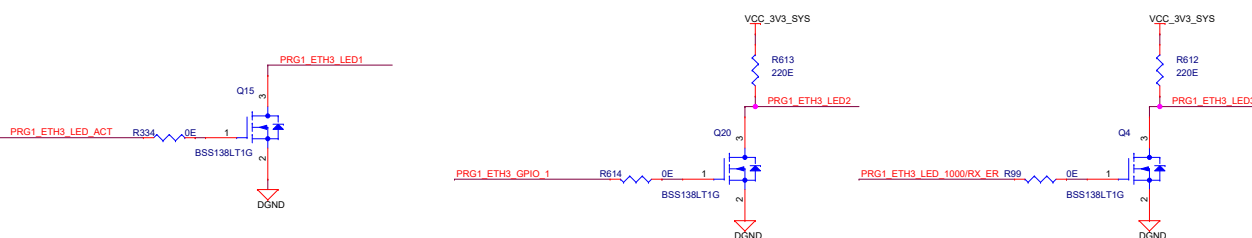
```
PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-T)
```



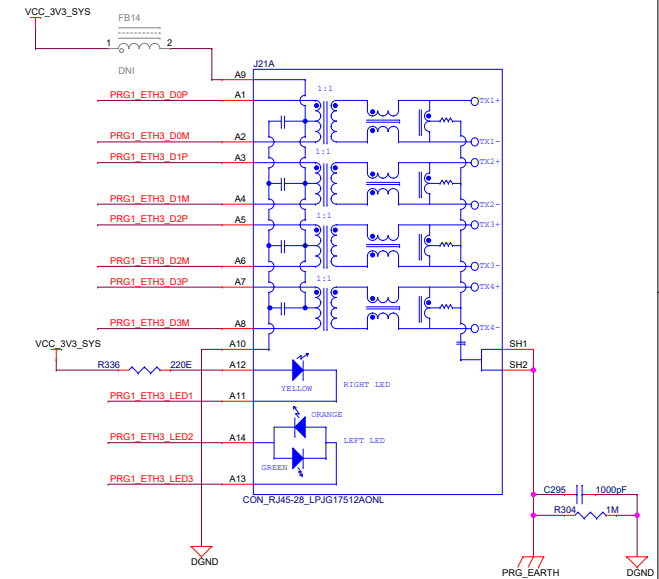
PRG1 ETH2 RESET



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

To Processor	16,17,34	PRG1_RGMII_INTn	↔	PRG1_RGMII_INTn
	27	PRG1_RGMII_RD0	↔	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	↔	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	↔	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	↔	PRG1_RGMII_RD3
	27	PRG1_RGMII_RX_CTL	↔	PRG1_RGMII_RX_CTL
	27	PRG1_RGMII_TX_CTL	↔	PRG1_RGMII_TX_CTL
	13,16,17,20,34	PORz_OUT	↔	PORz_OUT
	27	PRG1_ETH3_LED_LINK	↔	PRG1_ETH3_LED_LINK
	27	PRG1_ETH3_LED_1000RX_ER	↔	PRG1_ETH3_LED_1000RX_ER
From Processor	27	PRG1_RGMII_TD0	↔	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	↔	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	↔	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	↔	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	↔	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	↔	PRG1_RGMII_TX_CTL
	27	PRG1_RGMII_TX_CTL	↔	PRG1_RGMII_TX_CTL
From Processor	17,27	PRG1_MDIO_MDIO	↔	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	↔	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII1_RST	↔	GPIO_RGMII1_RST
	31	PRG1_RGMII1_ETH3_CLK	↔	PRG1_RGMII1_ETH3_CLK

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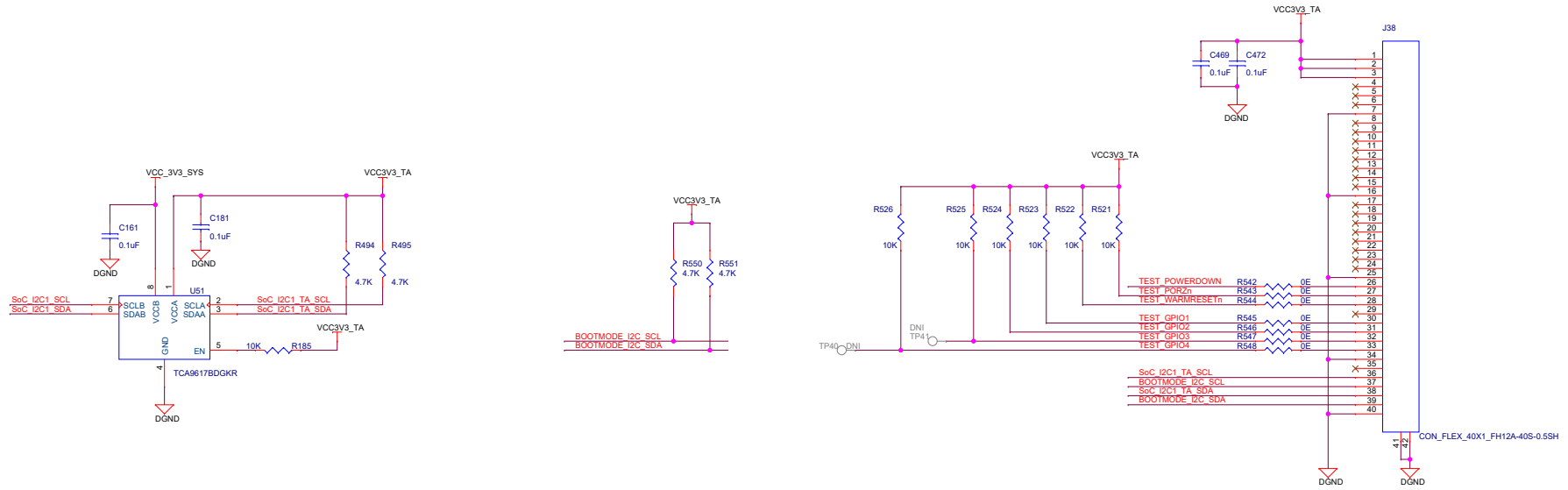


Title	ICSSG2 RGMII_1 ETHERNET PHY
-------	-----------------------------

Size	Variant Name = PROC101C(003) TMS64HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL	SoC_I2C1_SCL
	15,21,29,30,31,32,33	SoC_I2C1_SDA	SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

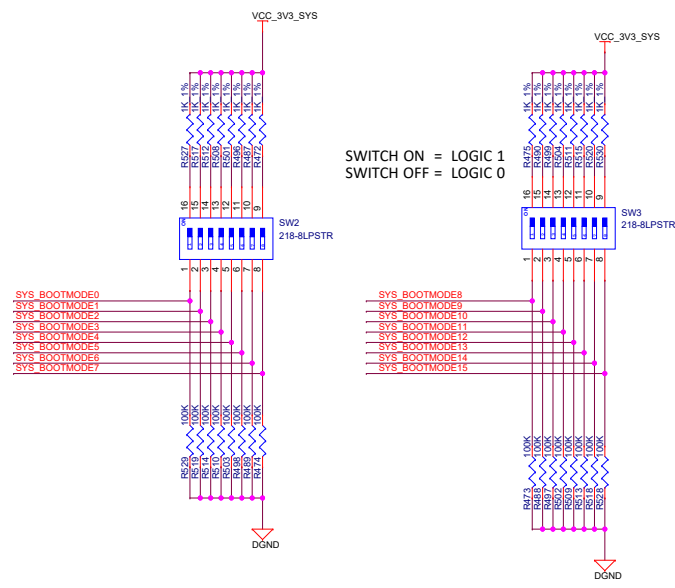
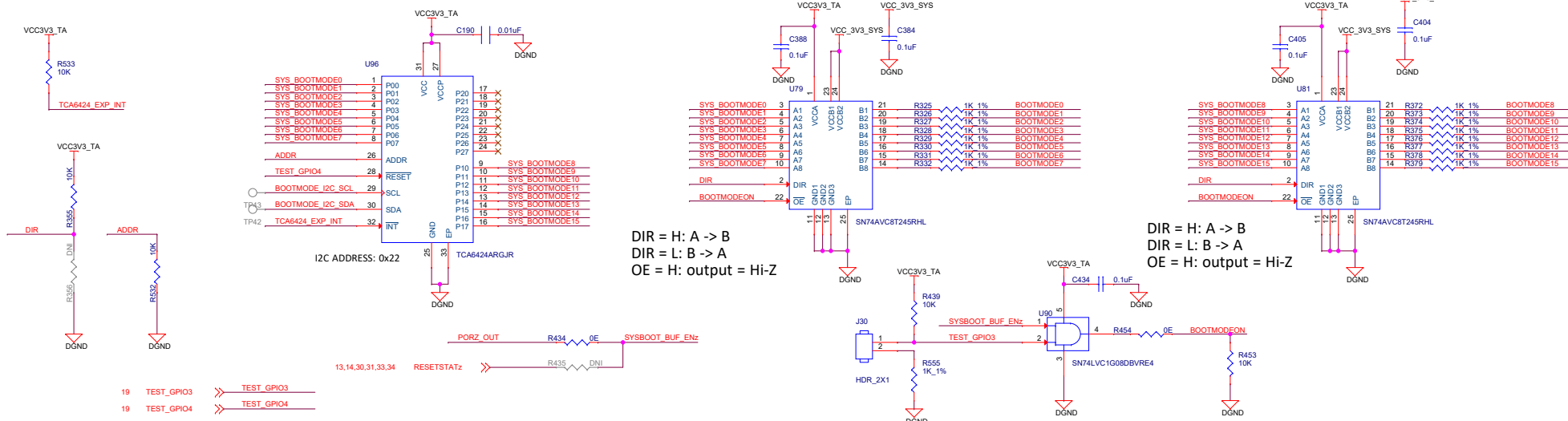
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Title TEST AUTOMATION

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 19 of 40

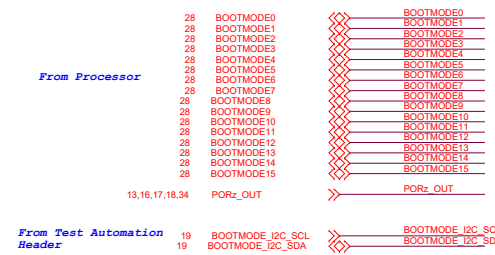
BOOT MODE BUFFER & SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections



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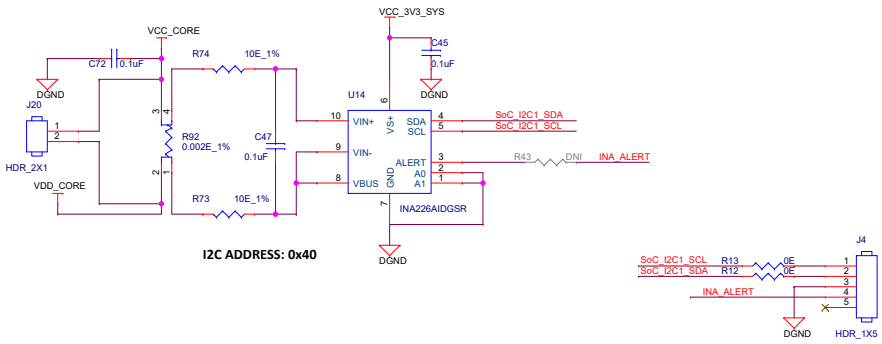


Title BOOT MODE BUFFER & SWITCHES

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 20 of 40

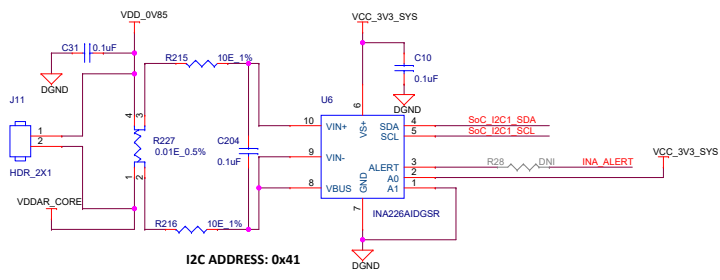
CURRENT MONITORING DEVICES

VDD_CORE



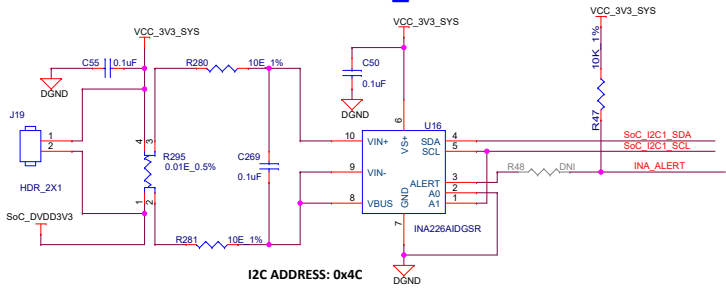
I2C ADDRESS: 0x40

VDDAR_CORE

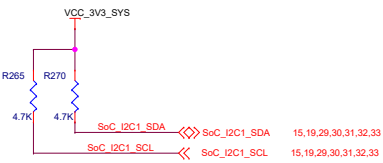


I2C ADDRESS: 0x41

SoC_DVDD3V3

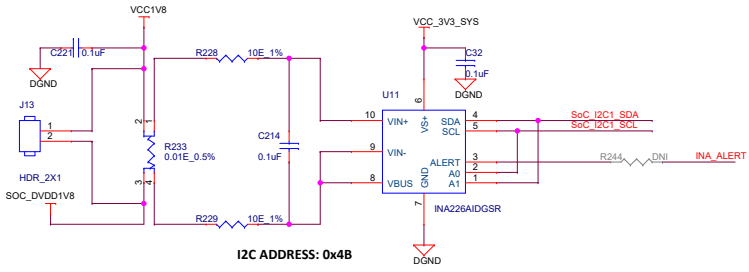


I2C ADDRESS: 0x4C



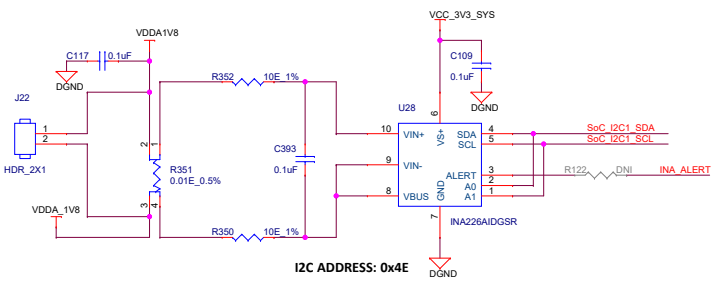
INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

SoC_DVDD1V8



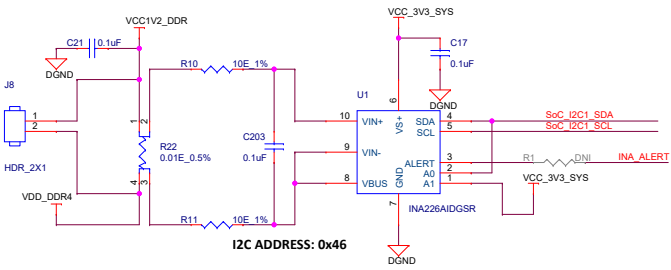
I2C ADDRESS: 0x4B

VDDA_1V8



I2C ADDRESS: 0x4E

VDD_DDR4



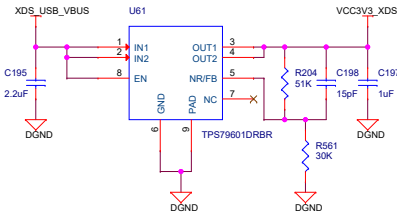
I2C ADDRESS: 0x46

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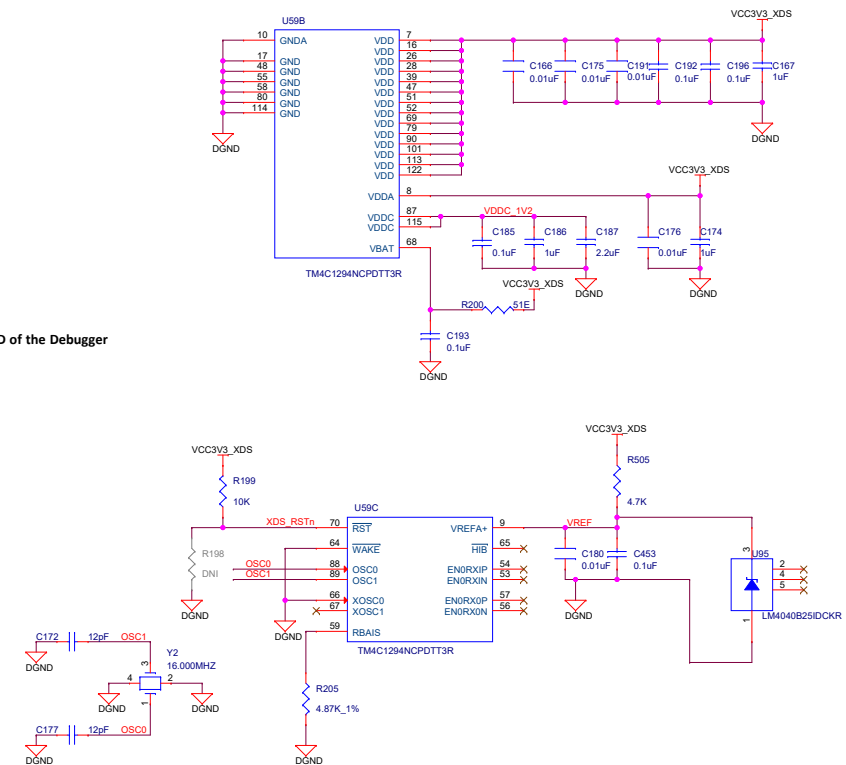
Title CURRENT MONITORING DEVICES		
Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 21 of 40

USB Connector



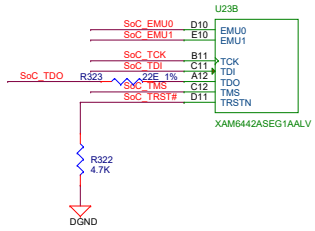
VCC3V3_XDS

R202
4.7K

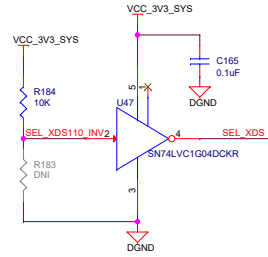


Size	Variant Name = PROC101C(003) TMS64HSEVM	Rev
C		E2
Date: Monday, August 22, 2022	Sheet 22 of 40	

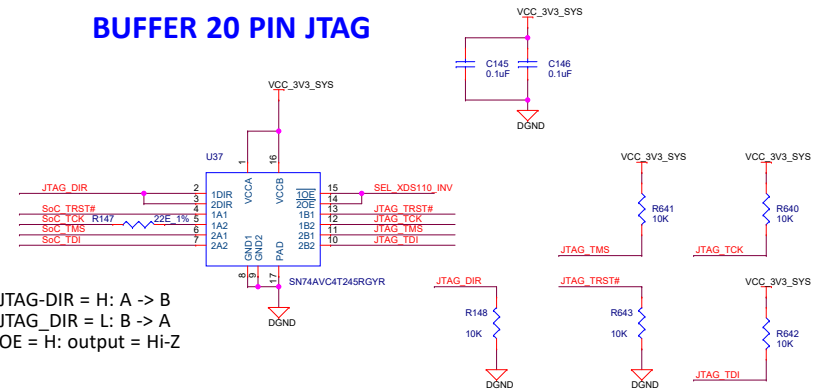
JTAG SoC SECTION



JTAG BUFFER

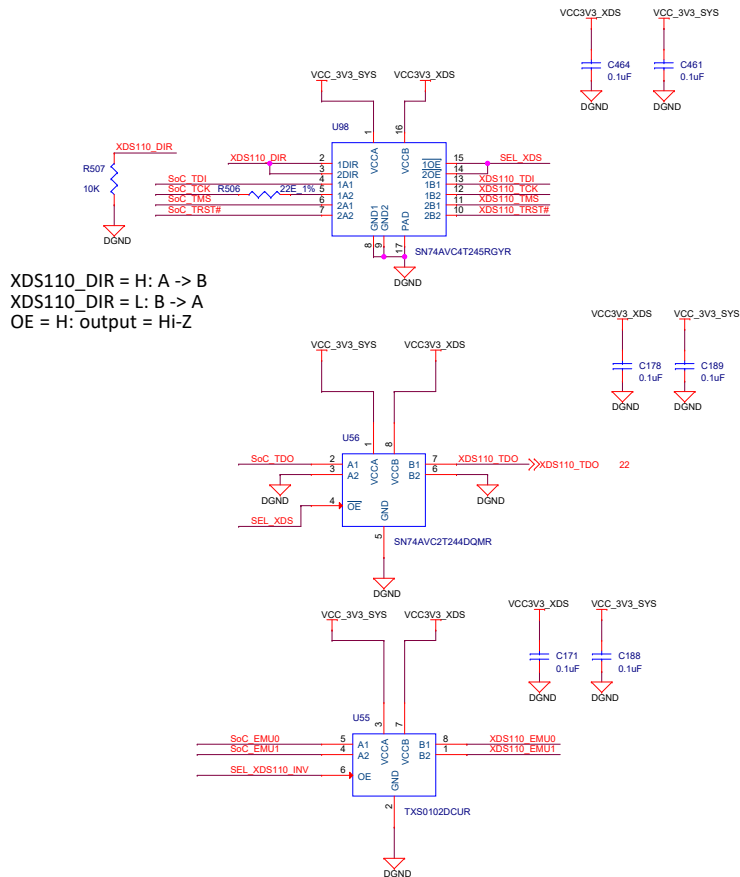


BUFFER 20 PIN JTAG



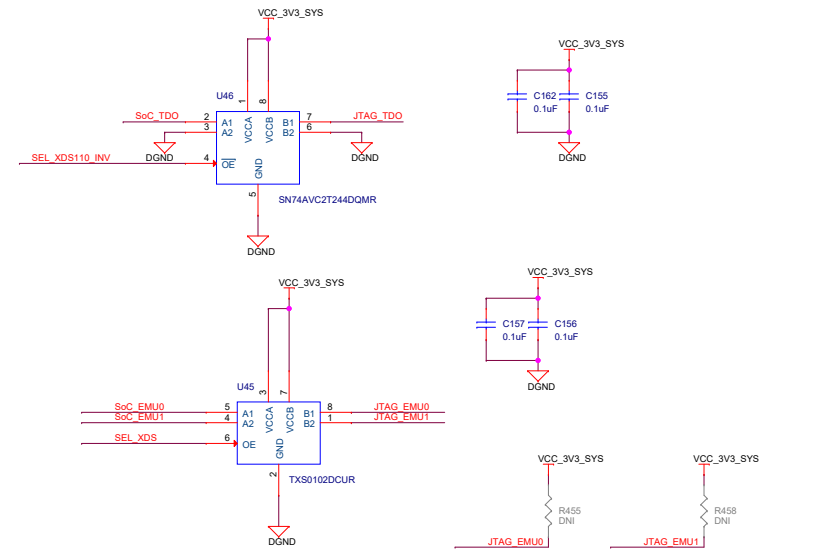
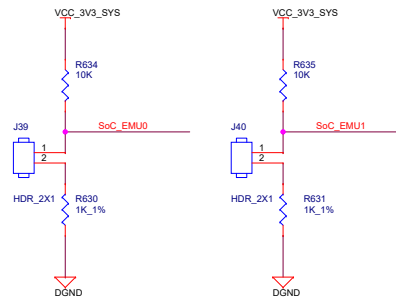
JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

BUFFER XDS110



XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25



Off Page Connections

From XDS1100 Debugger

24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TCK
22	XDS110_TCK	XDS110_TMS
22	XDS110_TMS	XDS110_TRST#
22	XDS110_TRST#	JTAG_TDI
24	JTAG_TDI	JTAG_TCK
24	JTAG_TCK	JTAG_TMS
24	JTAG_TMS	JTAG_TRST#
24	JTAG_TRST#	JTAG_TDO
24	JTAG_TDO	XDS110_EMU0
22	XDS110_EMU0	XDS110_EMU1

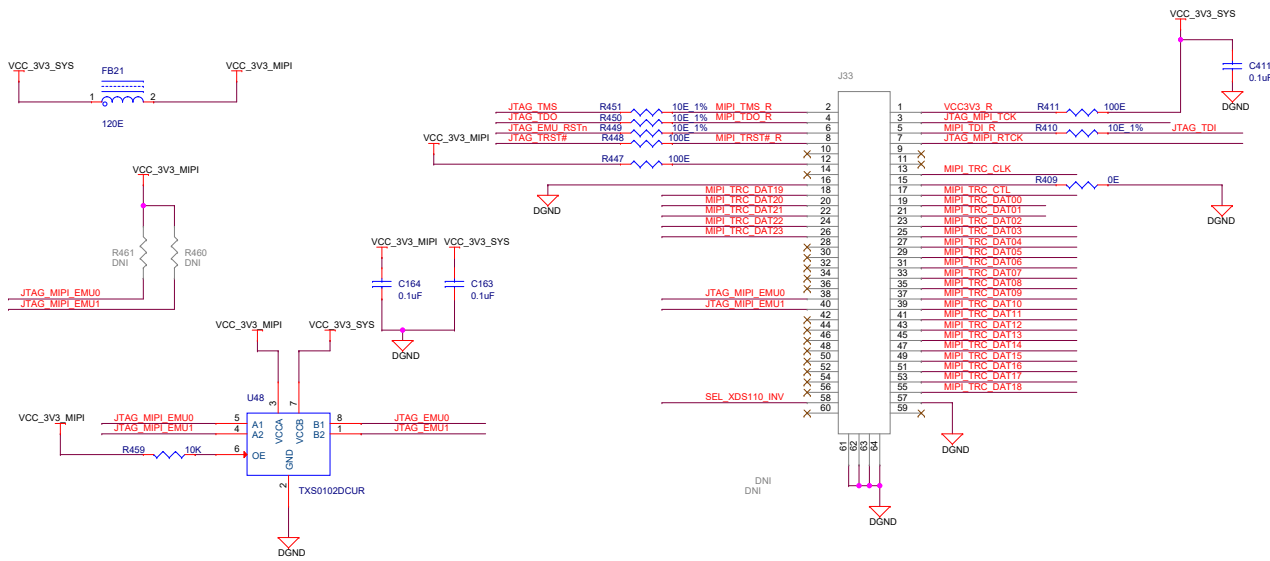
Designed for TI by Mistral Solutions Pvt Ltd



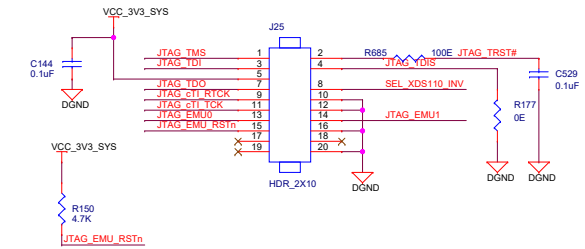
Title JTAG BUFFER

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 23 of 40

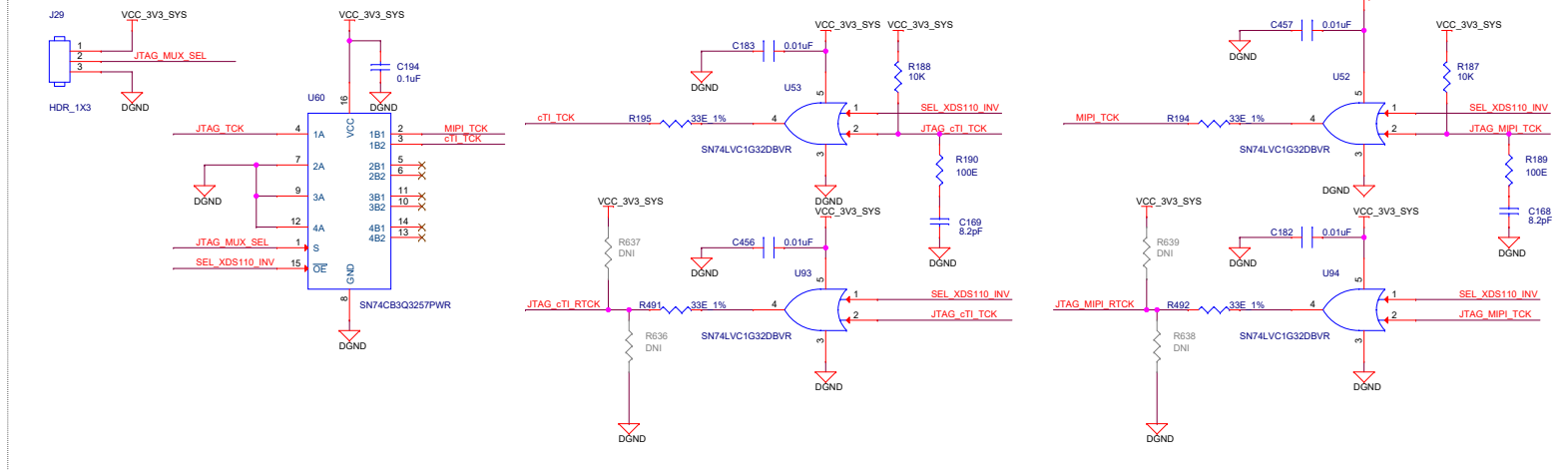
MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER

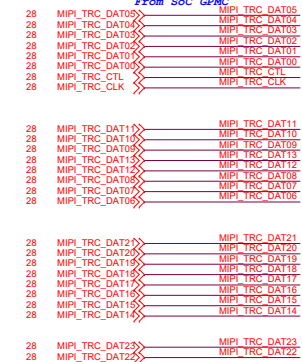


Off Page Connections

From JTAG Buffer



From SoC GPMC

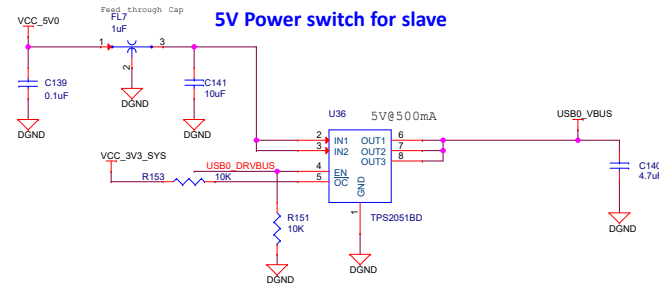
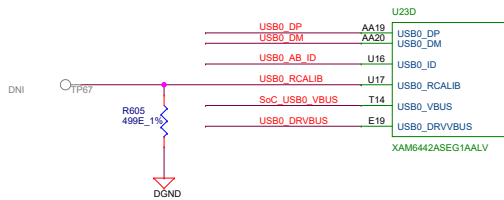


Designed for TI by Mistral Solutions Pvt Ltd

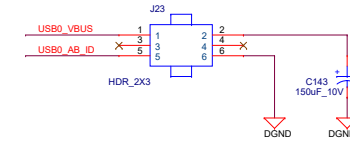


Title				MPII 60 PIN CONNECTOR			
Size		Variant Name = PROC101C(003) TMD564HSEVM				Rev	
C						E2	
Date:		Monday, August 22, 2022		Sheet		24 of 40	

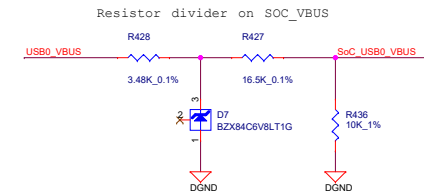
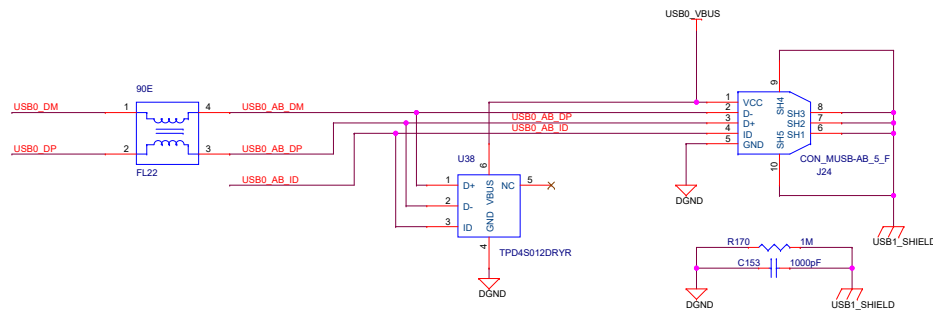
USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0_VBUS in host mode and to ground USB0_AB_ID pin, if a non standard cable is used



Micro USB 2.0 AB Connector



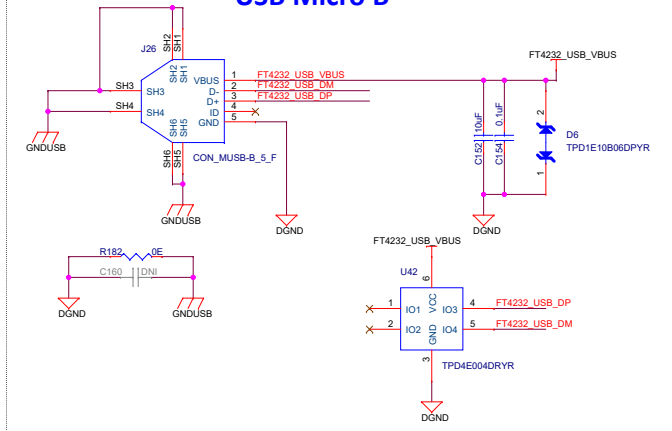
Designed for TI by Mistral Solutions Pvt Ltd



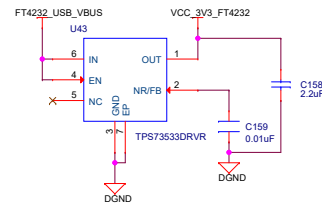
Title: USB 2.0 INTERFACE

Size	Variant Name = PROC101C(003) TMD684HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 25 of 40

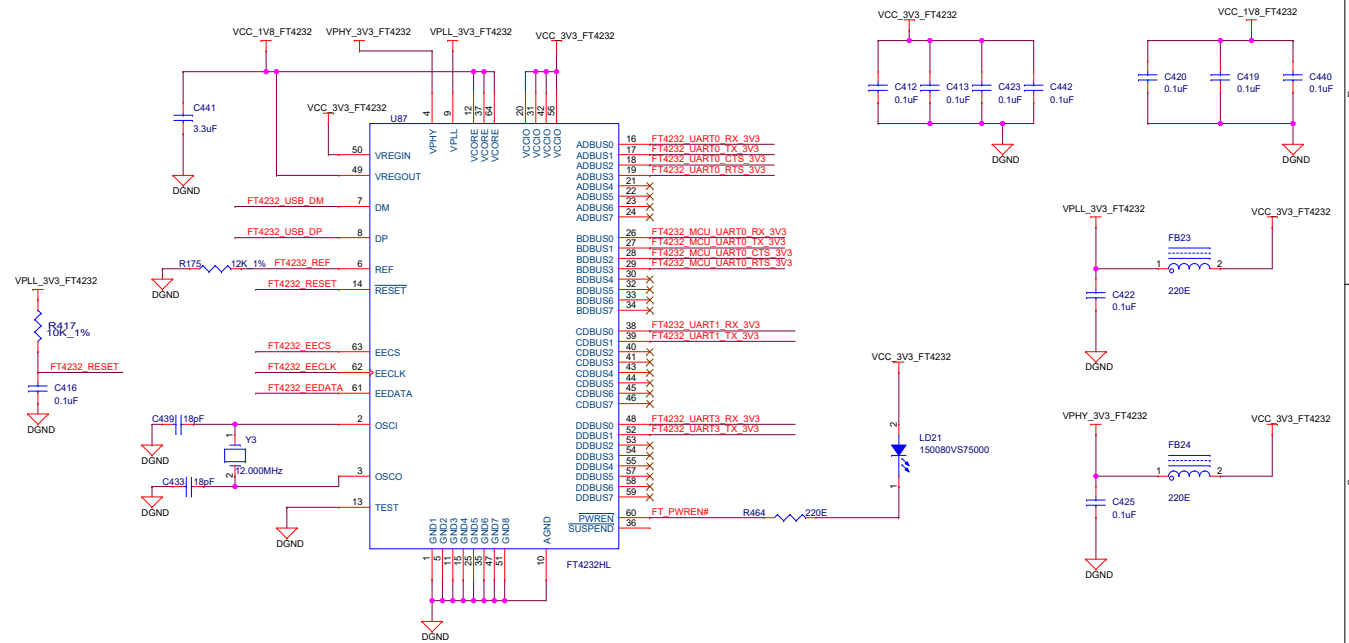
USB Micro B



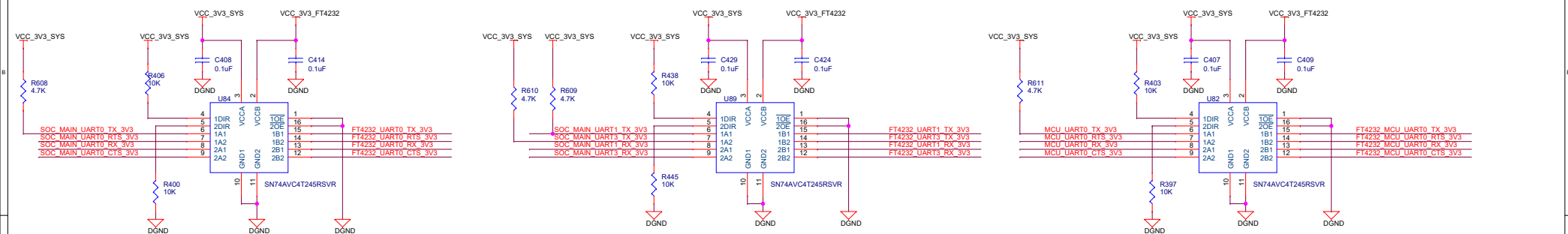
FT4232: 5V to 3.3V@500mA LDO



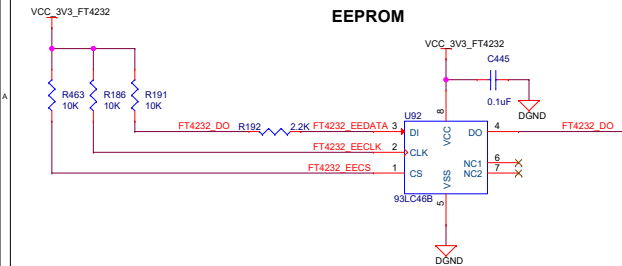
FT4232 UART



FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	SOC_MAIN_UART1_CTS_3V3	29

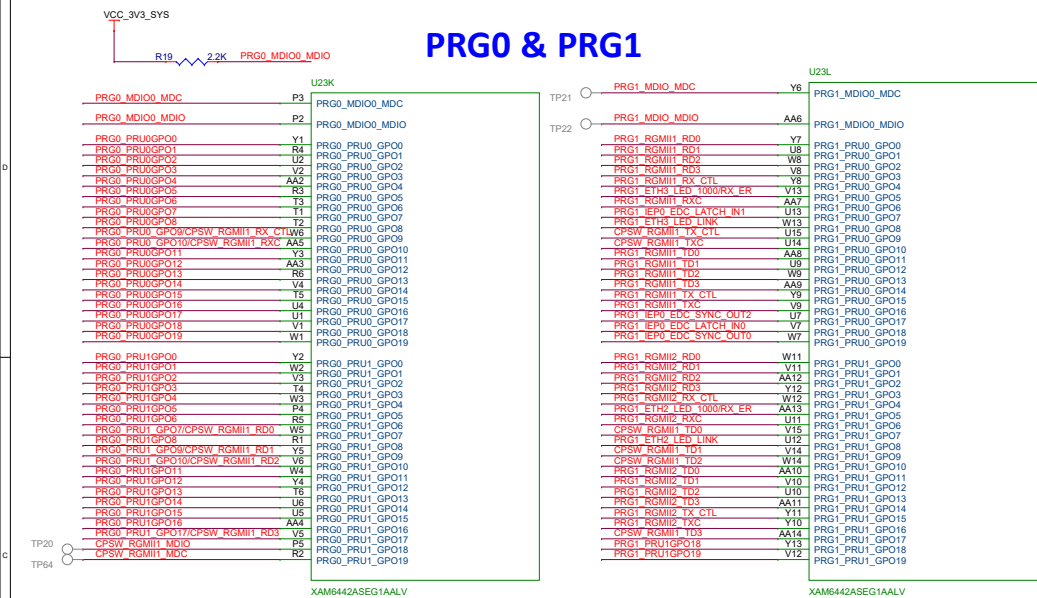
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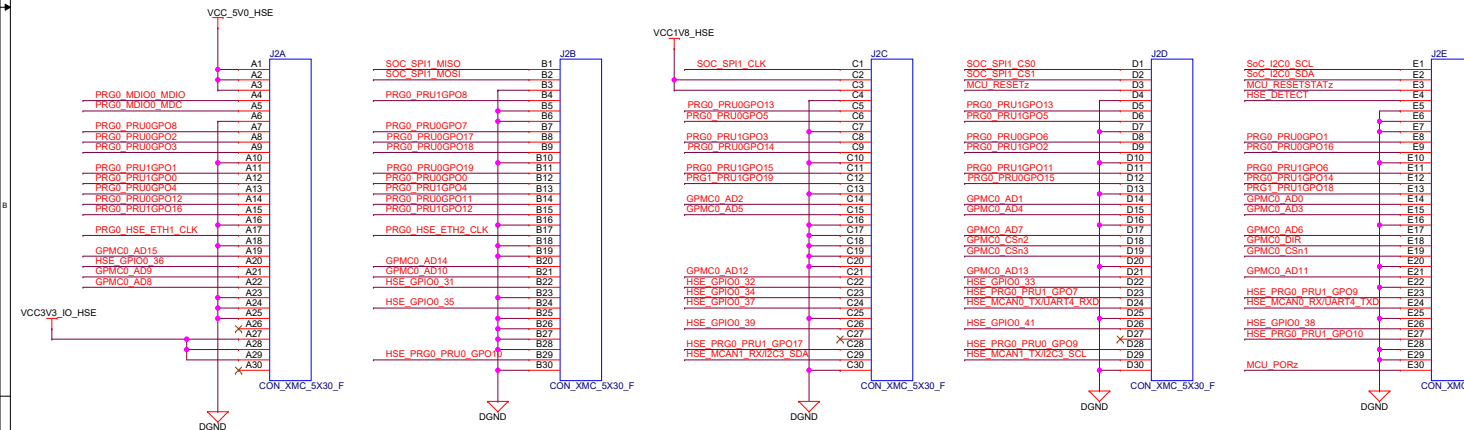
Title FT4232 UART to USB BRIDGE

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 26 of 40

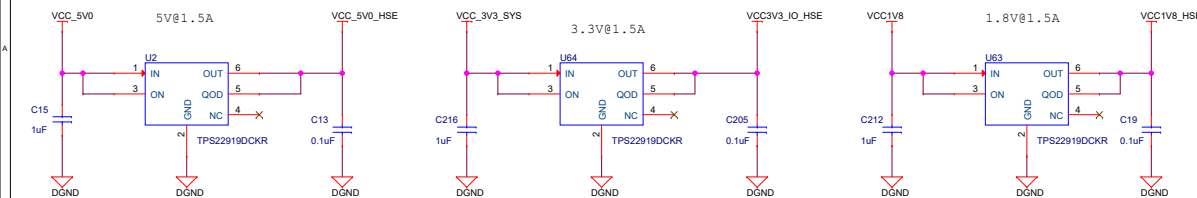
PRG0 & PRG1



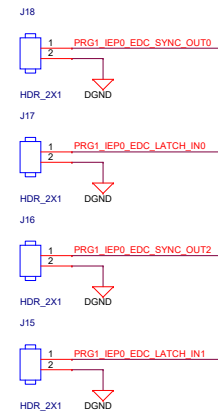
HIGH SPEED EXPANSION CONNECTOR



HSE CONNECTOR LOAD SWITCHES



SYNC TP



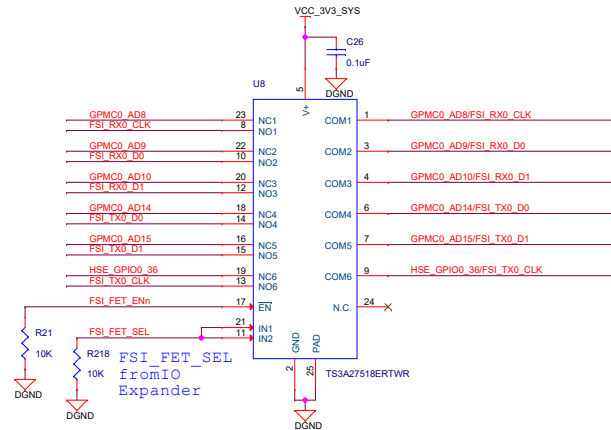
Off Page Connections

To Presence Detect Buffer	15	HSE_DETECT	<<	HSE_DETECT
From Processor GPMC	28	GPIMCO_CSn1	<<	GPIMCO_CSn1
	28	GPIMCO_CSn2	<<	GPIMCO_CSn2
	28	GPIMCO_CSn3	<<	GPIMCO_CSn3
	28	GPIMCO_DIR	<<	GPIMCO_DIR
From FSI mux	28	GPIMCO_A08	<<	GPIMCO_A08
	28	GPIMCO_A09	<<	GPIMCO_A09
	28	GPIMCO_A10	<<	GPIMCO_A10
	28	GPIMCO_A14	<<	GPIMCO_A14
	28	GPIMCO_AD15	<<	GPIMCO_AD15
	28	HSE_GP100_36	<<	HSE_GP100_36
From Processor GPMC resistor muxed with MIP1	28	GPIMCO_A00	<<	GPIMCO_A00
	28	GPIMCO_A01	<<	GPIMCO_A01
	28	GPIMCO_A02	<<	GPIMCO_A02
	28	GPIMCO_A03	<<	GPIMCO_A03
	28	GPIMCO_A04	<<	GPIMCO_A04
	28	GPIMCO_A05	<<	GPIMCO_A05
	28	GPIMCO_A06	<<	GPIMCO_A06
	28	GPIMCO_A07	<<	GPIMCO_A07
	28	GPIMCO_A11	<<	GPIMCO_A11
	28	GPIMCO_A12	<<	GPIMCO_A12
	28	GPIMCO_A13	<<	GPIMCO_A13
	28	HSE_GP100_37	<<	HSE_GP100_37
	28	HSE_GP100_38	<<	HSE_GP100_38
	28	HSE_GP100_39	<<	HSE_GP100_39
	28	HSE_GP100_40	<<	HSE_GP100_40
From Processor	34	MCU_PORz	<<	MCU_PORz
	34,35	MCU_RESETz	<<	MCU_RESETzTz
	34	MCU_RESETzTz	<<	MCU_RESETzTz
	29	HSE_MCAN0_RXUIAT4_TXD	<<	HSE_MCAN0_RXUIAT4_TXD
	29	HSE_MCAN0_RXUIAT4_RXD	<<	HSE_MCAN0_RXUIAT4_RXD
	29	HSE_MCAN1_RXUIAT3_SCL	<<	HSE_MCAN1_RXUIAT3_SCL
	29	HSE_MCAN1_TXUIAT3_SCL	<<	HSE_MCAN1_TXUIAT3_SCL
	29	SOC_SPH1_CLK	<<	SOC_SPH1_CLK
	29	SOC_SPH1_M0S0	<<	SOC_SPH1_M0S0
	29	SOC_SPH1_M0S1	<<	SOC_SPH1_M0S1
	29	SOC_SPH1_M0S2	<<	SOC_SPH1_M0S2
	29	SOC_SPH1_CST1	<<	SOC_SPH1_CST1
	15,29,33	Soc_I2C0_SCL	<<	Soc_I2C0_SCL
	15,29,33	Soc_I2C0_SDA	<<	Soc_I2C0_SDA
From clock Buffer	31	PRG0_HSE_ETH1_CLK	<<	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	<<	PRG0_HSE_ETH2_CLK
To and from ICSSG1 RGMII 2 Ethernet PHY	17	PRG1_RGMII2_RD0	<<	PRG1_RGMII2_RD0
	17	PRG1_RGMII2_RD1	<<	PRG1_RGMII2_RD1
	17	PRG1_RGMII2_RD2	<<	PRG1_RGMII2_RD2
	17	PRG1_RGMII2_RD3	<<	PRG1_RGMII2_RD3
	17	PRG1_RGMII2_RXC	<<	PRG1_RGMII2_RXC
	17	PRG1_RGMII2_RX_CTL	<<	PRG1_RGMII2_RX_CTL
	17	PRG1_ETH2_LED_1000RX_ER	<<	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMII2_TD0	<<	PRG1_RGMII2_TD0
	17	PRG1_RGMII2_TD1	<<	PRG1_RGMII2_TD1
	17	PRG1_RGMII2_TD2	<<	PRG1_RGMII2_TD2
	17	PRG1_RGMII2_TD3	<<	PRG1_RGMII2_TD3
	17	PRG1_RGMII2_TXC	<<	PRG1_RGMII2_TXC
	17	PRG1_RGMII2_TX_CTL	<<	PRG1_RGMII2_TX_CTL
	17,18	PRG1_MDIO_MDIO	<<	PRG1_MDIO_MDIO
	17,18	PRG1_ETH3_LED_LINK	<<	PRG1_ETH3_LED_LINK
To and from ICSSG2 RGMII 1 Ethernet PHY	17	PRG1_ETH2_LED_LINK	<<	PRG1_ETH2_LED_LINK
	18	PRG1_RGMII1_RD0	<<	PRG1_RGMII1_RD0
	18	PRG1_RGMII1_RD1	<<	PRG1_RGMII1_RD1
	18	PRG1_RGMII1_RD2	<<	PRG1_RGMII1_RD2
	18	PRG1_RGMII1_RD3	<<	PRG1_RGMII1_RD3
	18	PRG1_RGMII1_RXC	<<	PRG1_RGMII1_RXC
	18	PRG1_RGMII1_RX_CTL	<<	PRG1_RGMII1_RX_CTL
	18	PRG1_ETH3_LED_1000RX_ER	<<	PRG1_ETH3_LED_1000RX_ER
	18	PRG1_RGMII1_TD0	<<	PRG1_RGMII1_TD0
	18	PRG1_RGMII1_TD1	<<	PRG1_RGMII1_TD1
	18	PRG1_RGMII1_TD2	<<	PRG1_RGMII1_TD2
	18	PRG1_RGMII1_TD3	<<	PRG1_RGMII1_TD3
	18	PRG1_RGMII1_TXC	<<	PRG1_RGMII1_TXC
	18	PRG1_RGMII1_TX_CTL	<<	PRG1_RGMII1_TX_CTL
From MUX To HSE	16	HSE_PRG0_PRU1_GP07	<<	HSE_PRG0_PRU1_GP07
	16	HSE_PRG0_PRU1_GP09	<<	HSE_PRG0_PRU1_GP09
	16	HSE_PRG0_PRU1_GP010	<<	HSE_PRG0_PRU1_GP010
	16	HSE_PRG0_PRU1_GP017	<<	HSE_PRG0_PRU1_GP017
	16	HSE_PRG0_PRU0_GP09	<<	HSE_PRG0_PRU0_GP09
	16	HSE_PRG0_PRU0_GP010	<<	HSE_PRG0_PRU0_GP010
	16,17	CPSW_RGMII1_MDIO	<<	CPSW_RGMII1_MDIO
	16,17	CPSW_RGMII1_MD0	<<	CPSW_RGMII1_MD0
To MUX From SoC	16	PRG0_PRU1_GP07/CPSW_RGMII1_RD0	<<	PRG0_PRU1_GP07/CPSW_RGMII1_RD0
	16	PRG0_PRU1_GP09/CPSW_RGMII1_RD1	<<	PRG0_PRU1_GP09/CPSW_RGMII1_RD1
	16	PRG0_PRU1_GP010/CPSW_RGMII1_RD2	<<	PRG0_PRU1_GP010/CPSW_RGMII1_RD2
	16	PRG0_PRU1_GP017/CPSW_RGMII1_RD3	<<	PRG0_PRU1_GP017/CPSW_RGMII1_RD3
	16	PRG0_PRU0_GP09/CPSW_RGMII1_RX_CTL	<<	PRG0_PRU0_GP09/CPSW_RGMII1_RX_CTL
	16	PRG0_PRU0_GP010/CPSW_RGMII1_RXC	<<	PRG0_PRU0_GP010/CPSW_RGMII1_RXC
From CPSW RGMII 1 PHY	16	CPSW_RGMII1_TD0	<<	CPSW_RGMII1_TD0
	16	CPSW_RGMII1_TD1	<<	CPSW_RGMII1_TD1
	16	CPSW_RGMII1_TD2	<<	CPSW_RGMII1_TD2
	16	CPSW_RGMII1_TD3	<<	CPSW_RGMII1_TD3
	16	CPSW_RGMII1_TXC	<<	CPSW_RGMII1_TXC
	16	CPSW_RGMII1_TX_CTL	<<	CPSW_RGMII1_TX_CTL

GPMC



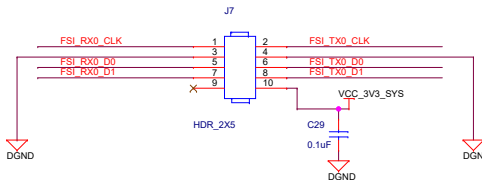
GPMC TO FSI & HSE CONNECTOR



TS3A27518ERTWR Truth Table

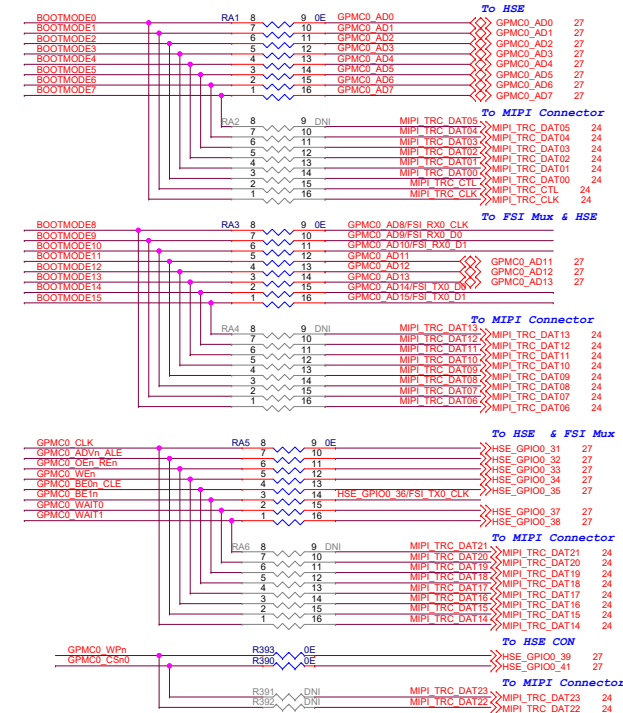
EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM1/2/3 & COM1/2/3 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

FSI CONNECTOR

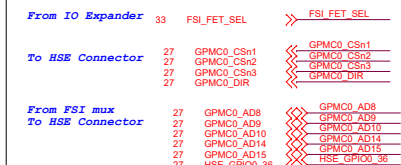


0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391 & R392 Should be DNI'd.
-For TRACE RA2, RA4, RA6, R391 & R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



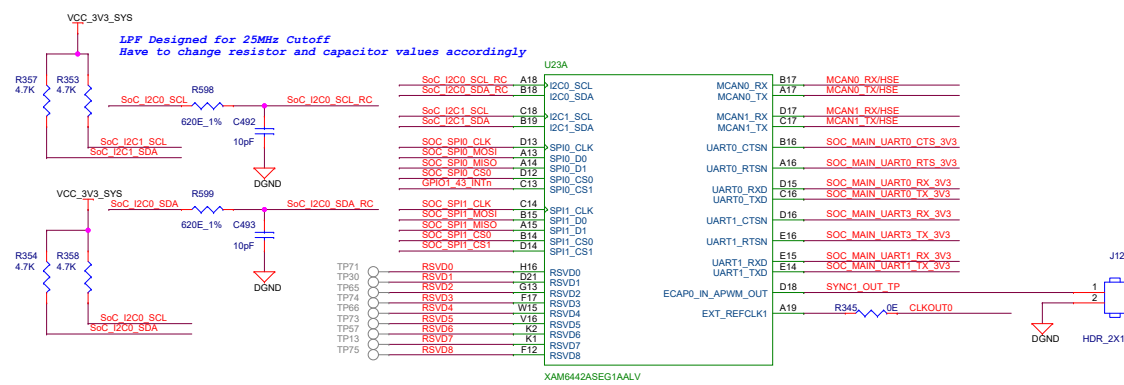
Off Page Connections



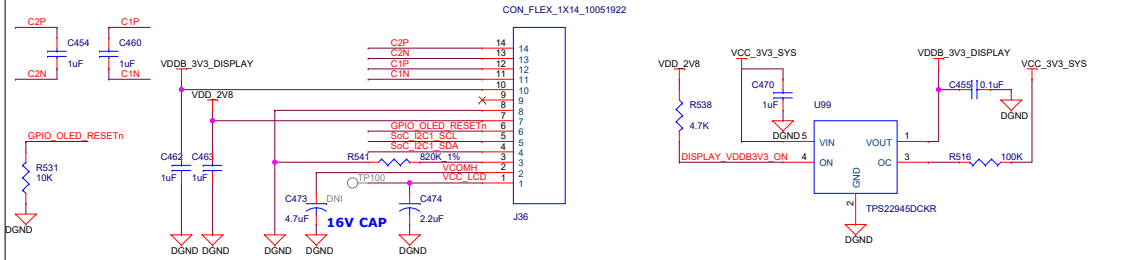
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Title		GPMC	
Size	Variant Name = PROC101C(003) TMD564HSEVM		Rev
C	Monday, August 22, 2022		E2
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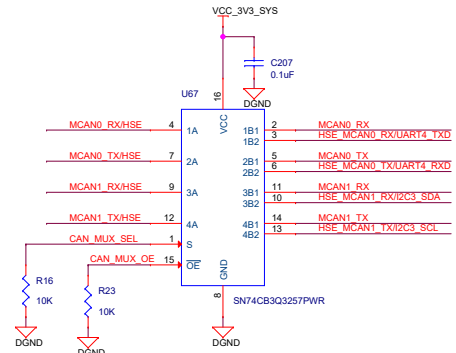
DISPLAY CONNECTOR



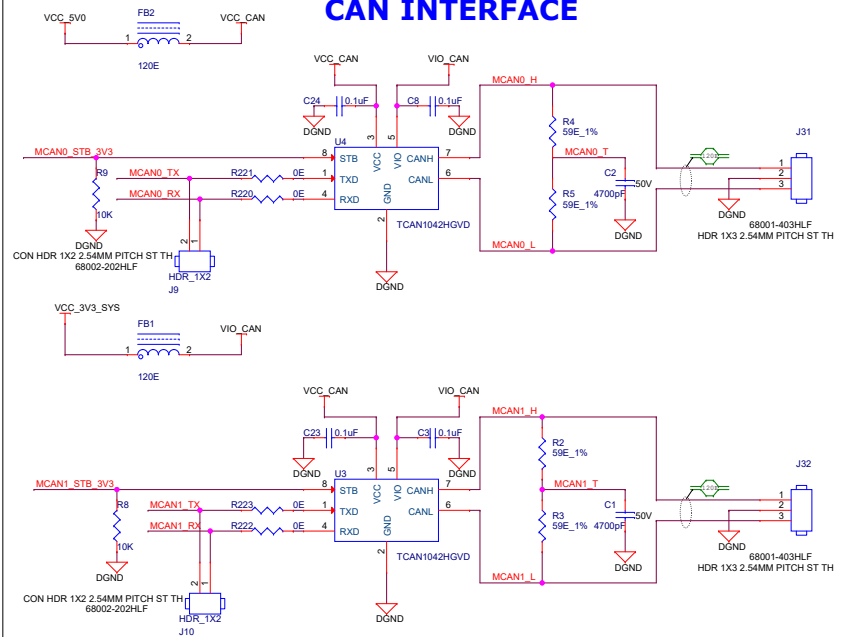
DISPLAY



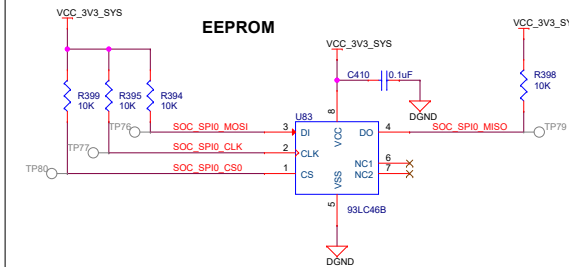
HSE/CAN MUX



CAN INTERFACE



SPI EEPROM



Off Page Connections

From Debounce Circuit	GPIO1_43_INn	35
From IO Expander	GPIO_OLED_RESETn	33
From HSE Connector	MCAN0_STB_3V3	33
	MCAN0_TXHSE	33
	MCAN0_TX	27
	MCAN0_RX	27
	MCAN1_TXHSE	27
	MCAN1_TX	27
	MCAN1_RX	27
	MCAN1_TX/UART3_SDA	27
	MCAN1_TX/UART3_SCL	27
	SOC_SPI0_CLK	27
	SOC_SPI0_MISO	27
	SOC_SPI0_CS0	27
	SOC_SPI1_CLK	27
	SOC_SPI1_MISO	27
	SOC_SPI1_CS0	27
	SOC_SPI1_CS1	27
	SOC_I2C0_SCL	15,27,33
	SOC_I2C0_SDA	15,27,33
	SOC_I2C1_SCL	15,19,21,30,31,32,33
	SOC_I2C1_SDA	15,19,21,30,31,32,33
	CLKOUT0	31
From Clock Buffer	SOC_MAIN_UART0_TX_3V3	26
	SOC_MAIN_UART0_CTS_3V3	26
	SOC_MAIN_UART0_RTS_3V3	26
	SOC_MAIN_UART0_RX_3V3	26
From FT4232 Bridge	SOC_MAIN_UART1_TX_3V3	26
	SOC_MAIN_UART1_RX_3V3	26
	SOC_MAIN_UART3_TX_3V3	26
	SOC_MAIN_UART3_RX_3V3	26

PROC101C(003) TMD564HSEVM

Project :

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<Project Name>



Title

CAN & DISPLAY INTERFACE

Size

Document Number

C

MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA

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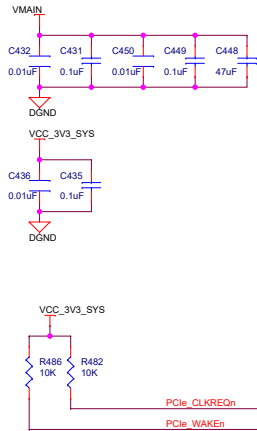
of

40

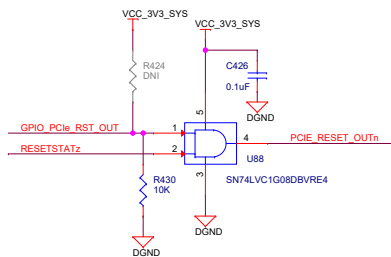
Rev

E2

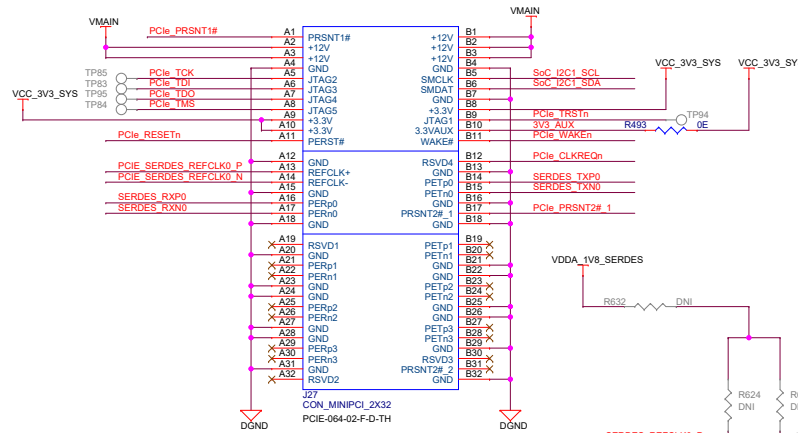
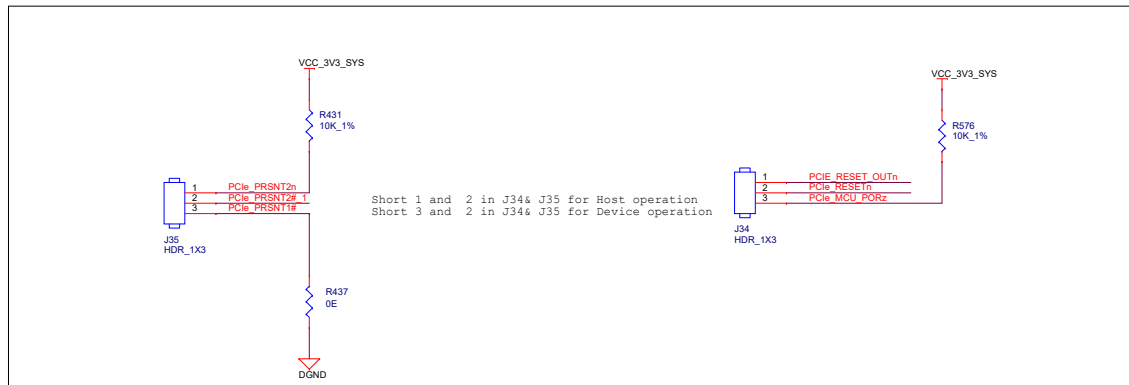
x4 Lane PCIe Connector



PCIe Reset

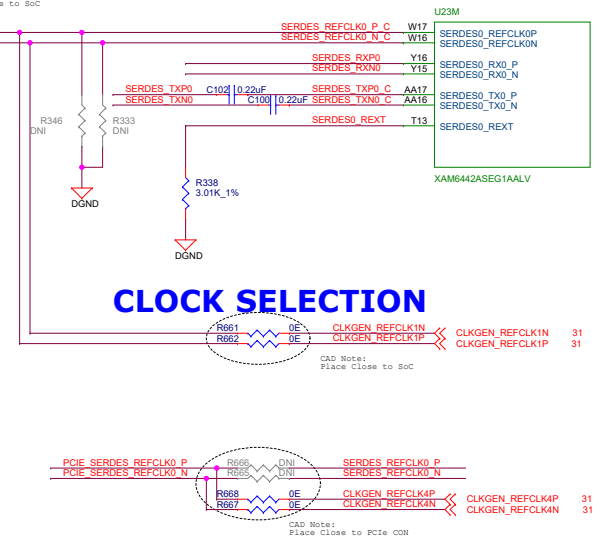


RC OR EP MODE SELECTION



Note:
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

CLOCK SELECTION



Off Page Connections

PCIE_MCU_PORz	PCIE_MCU_PORz	34
GPIO_Pcie_RST_OUT	GPIO_Pcie_RST_OUT	33
RESESTATz	RESESTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

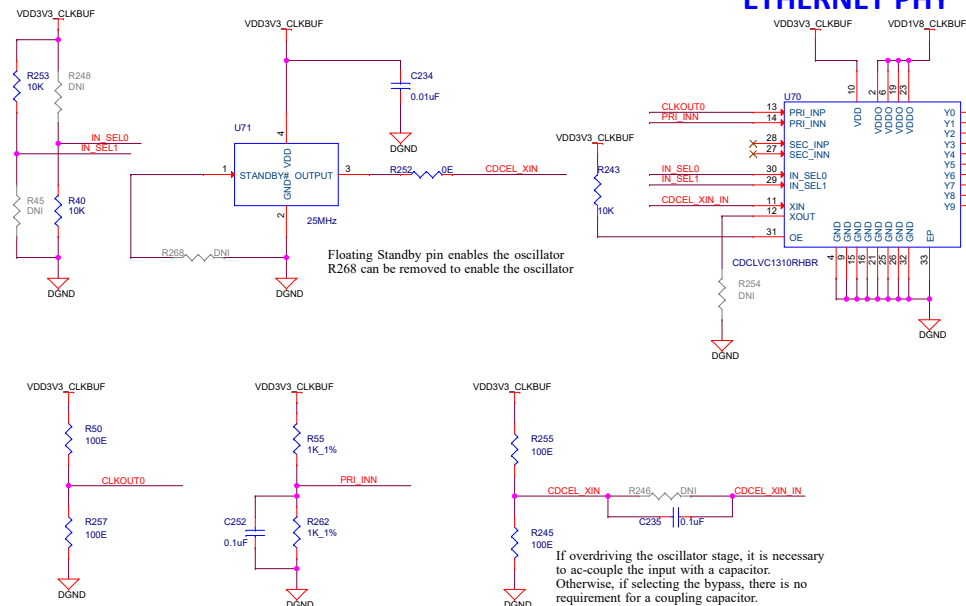
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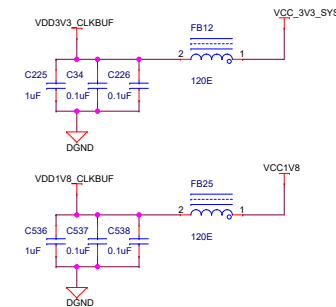
Title		
PCIe INTERFACE		
Size	PROC101C(003) TMD84HSEVM	Rev
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REFERENCE INPUT SELECTION

ETHERNET PHY CLOCK BUFFER



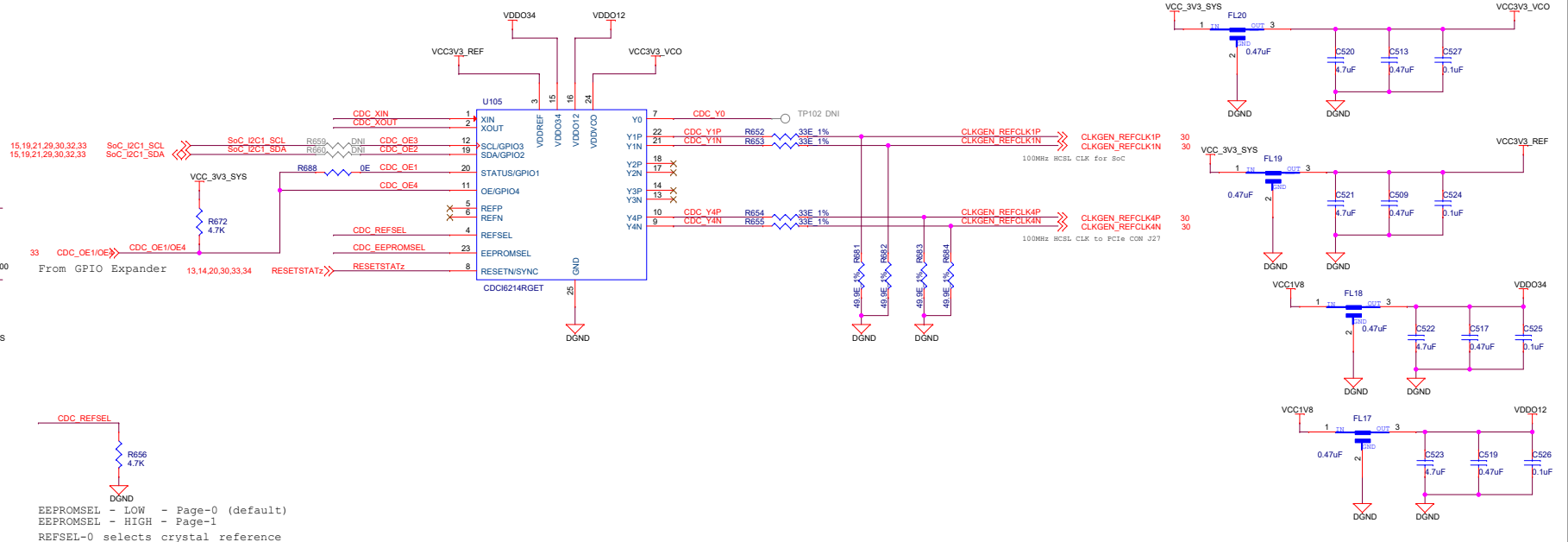
PROVIDING 2 CLOCK FOR HSE



Off Page Connections

From SoC CLKOUT0 << CLKOUT0 29

PCIe Clock HCSL (100MHz)



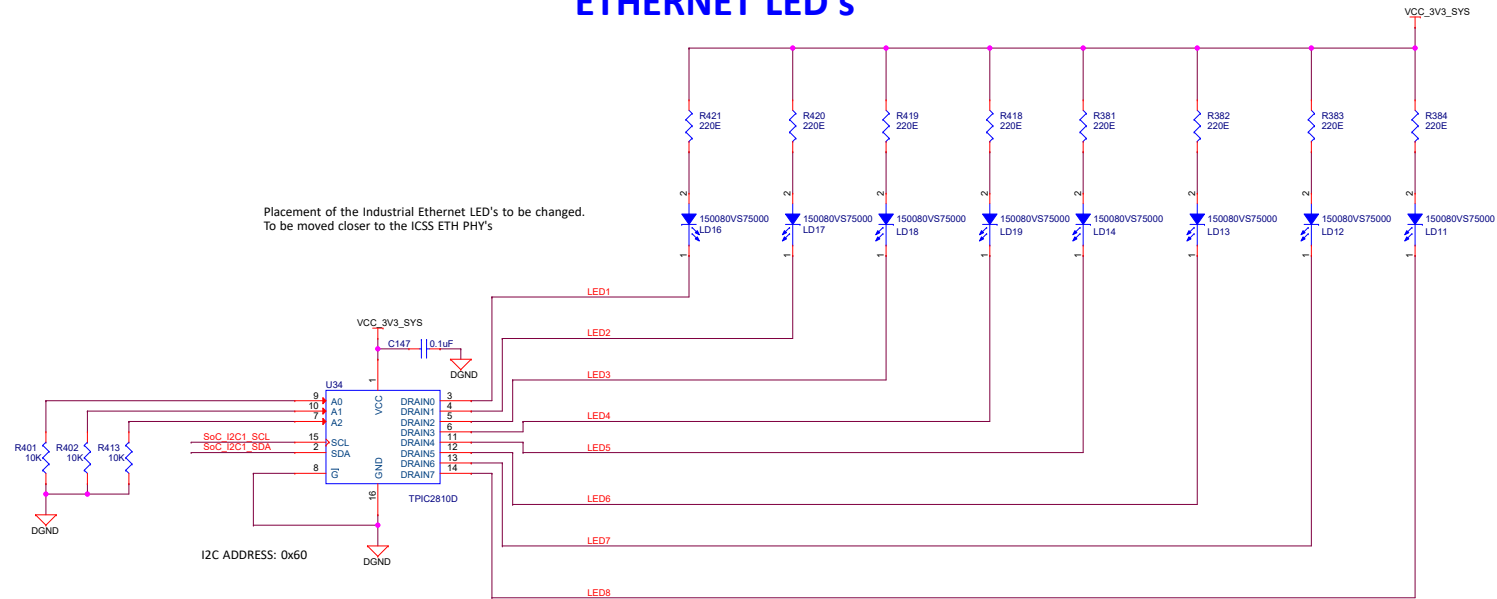
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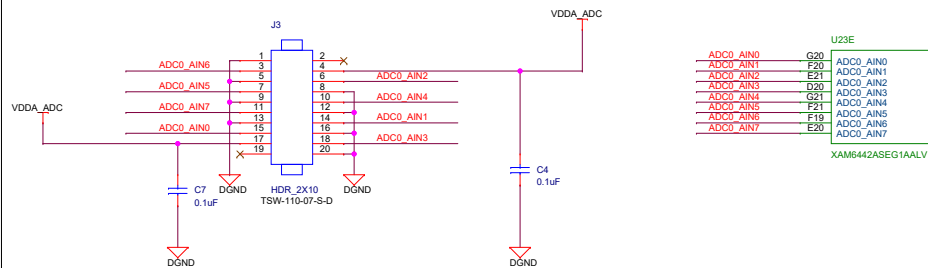
Title ETHERNET PHY & PCIe CLOCK GENERATOR

Size	Variant Name = PROC101C(003) TMD864HSEVM	Rev
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ETHERNET LED's



ADC CONNECTOR



Off Page Connections

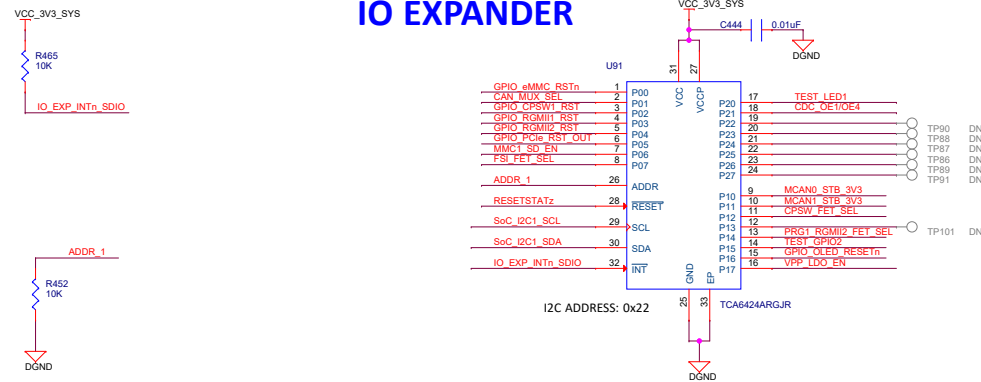
SoC_I2C1_SCL	15,19,21,29,30,31,33
SoC_I2C1_SDA	15,19,21,29,30,31,33

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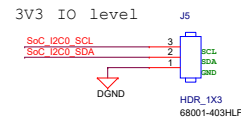


Title		ETHERNET LED's	
Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev	E2
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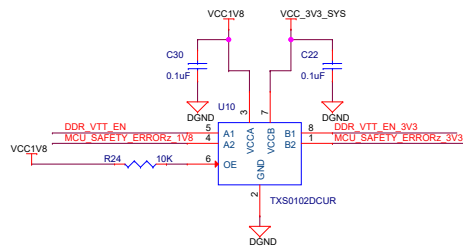
IO EXPANDER



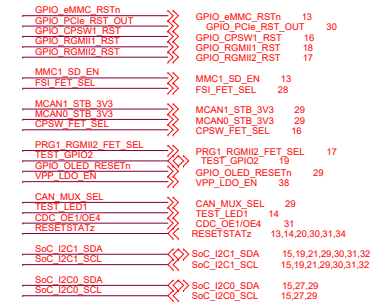
I2C TEST HEADER



LEVEL TRANSLATOR



Off Page Connections



From Safety Connector MCU SAFETY_ERRORz_3V3 MCU SAFETY_ERRORz_3V3 34

From SoC OSPI Section DDR_VTT_EN DDR_VTT_EN 14

To Processor MCU SAFETY_ERRORz_1V8 MCU SAFETY_ERRORz_1V8 34

To VTT Reg DDR_VTT_EN_3V3 DDR_VTT_EN_3V3 38

To SoC MMC IO_EXP_INTn_SDIO IO_EXP_INTn_SDIO 13

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Title IO EXPANDER

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
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The schematic diagram illustrates the MCU_GENERAL section, featuring two microcontrollers, U23H and U23C, and a comparator, SN74LVC1G11DCKR.

U23H Connections:

- MCU_I2C0_SCL_RC:** Connected to R309 (4.7K) and R311 (4.7K) to VCC_3V3_SYS.
- MCU_I2C0_SDA:** Connected to R303 (4.7K) and R306 (4.7K) to VCC_3V3_SYS.
- MCU_I2C1_SCL:** Connected to R303 (4.7K) and R306 (4.7K) to VCC_3V3_SYS.
- MCU_I2C1_SDA:** Connected to R303 (4.7K) and R306 (4.7K) to VCC_3V3_SYS.
- MCU_OSC0_XI:** Connected to C21 (620E_1%) and R302 (22E_1%) to VCC_3V3_SYS.
- MCU_OSC0_XO:** Connected to C21 (620E_1%) and R302 (22E_1%) to VCC_3V3_SYS.
- MCU_SPI0_CLK:** Connected to R593 (620E_1%) and C487 (10pF) to VCC_3V3_SYS.
- MCU_SPI0_D0:** Connected to R594 (620E_1%) and C488 (10pF) to VCC_3V3_SYS.
- MCU_SPI0_D1:** Connected to R594 (620E_1%) and C488 (10pF) to VCC_3V3_SYS.
- MCU_SPI0_CS0:** Connected to R594 (620E_1%) and C488 (10pF) to VCC_3V3_SYS.
- MCU_SPI0_CS1:** Connected to R594 (620E_1%) and C488 (10pF) to VCC_3V3_SYS.
- MCU_GPIO0_7:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_GPIO0_8:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_GPIO0_9:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- TEST_LED2:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_GPIO0_6:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART0_RX_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART0_TX_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART1_RX_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART1_TX_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART0_CTS_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART0_RTS_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART1_CTS_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.
- MCU_UART1_RTS_3V3:** Connected to R597 (620E_1%) and C491 (10pF) to VCC_3V3_SYS.

U23C Connections:

- PRG1_RGMII_INTn_RC:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- EXTINTN:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_SAFETY_ERRORn_1V8:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_PORz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- PORz_OUT:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_RESETz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_RESETSTATz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- RESET_REQz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- RESETSTATz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.

SN74LVC1G11DCKR Connections:

- VCC1V8:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_PORz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_RESETz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- MCU_RESETSTATz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- RESET_REQz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.
- RESETSTATz:** Connected to R574 (DNI) and C485 (0.1uF) to VCC1V8.

To HSE Connector	MCU_RESETSTATz	MCU_RESETz	27,35	
		MCU_RESETSTATz	27	
To level translator	MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3		33
From level translator	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8		33
To Boot Mode Section	PORz_OUT	PORz_OUT	13,16,17,18,20	
From ICSSG Phyl62	PRG1_RGMIIInTn	PRG1_RGMIIInTn	16,17,18	
To User LED	TEST_LED2	TEST_LED2	14	
From Push button	MCU_GPIO0_6	MCU_GPIO0_6	35	
Switch				
	SoC_CLKIN	SoC_CLKIN	31	
	MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26	
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26	
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26	
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26	

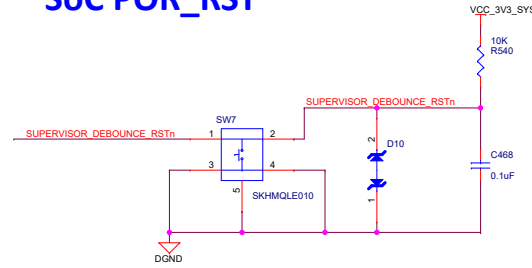
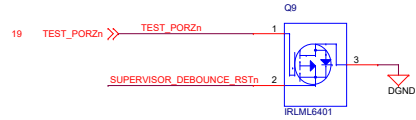


TEXAS
INSTRUMENTS

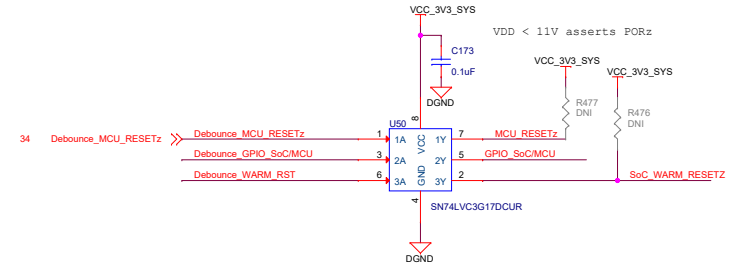


Size	Variant Name = PROC101C(003) TMSD64HSEVM	Rev
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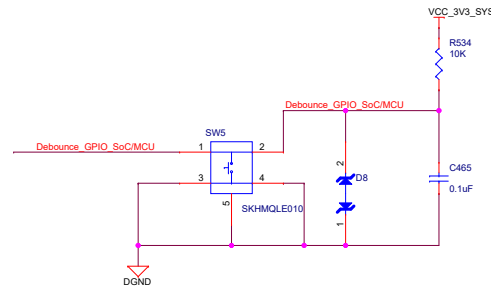
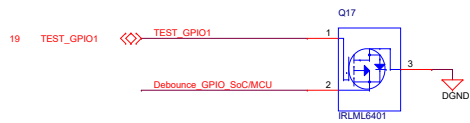
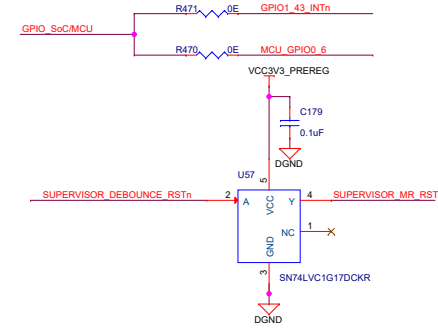
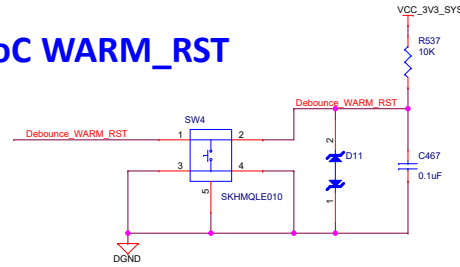
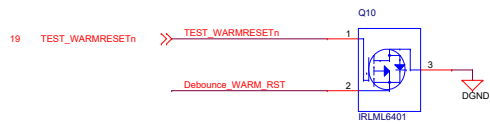
SoC POR_RST



DEBOUNCE CIRCUIT



SoC WARM_RST

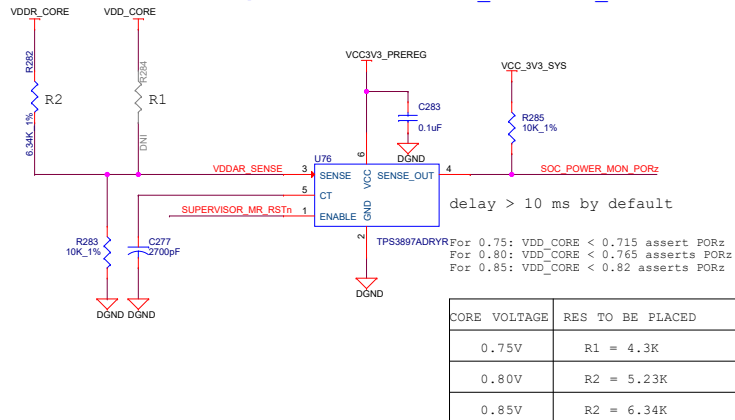


Off Page Connections

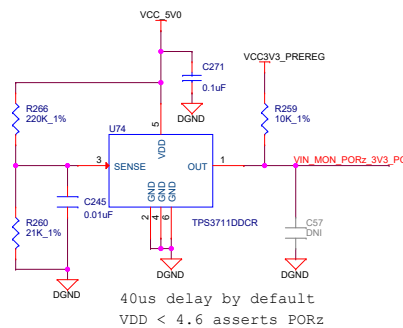
To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz	34
	GPIO1_43_INTn	GPIO1_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPIO0_6	MCU_GPIO0_6	34

VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



5V OUTPUT MONITOR (VCC_5V0)



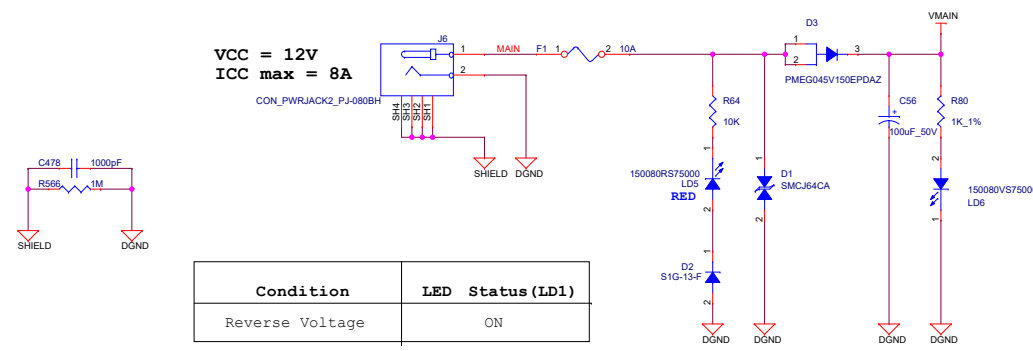
Designed for TI by Mistral Solutions Pvt Ltd



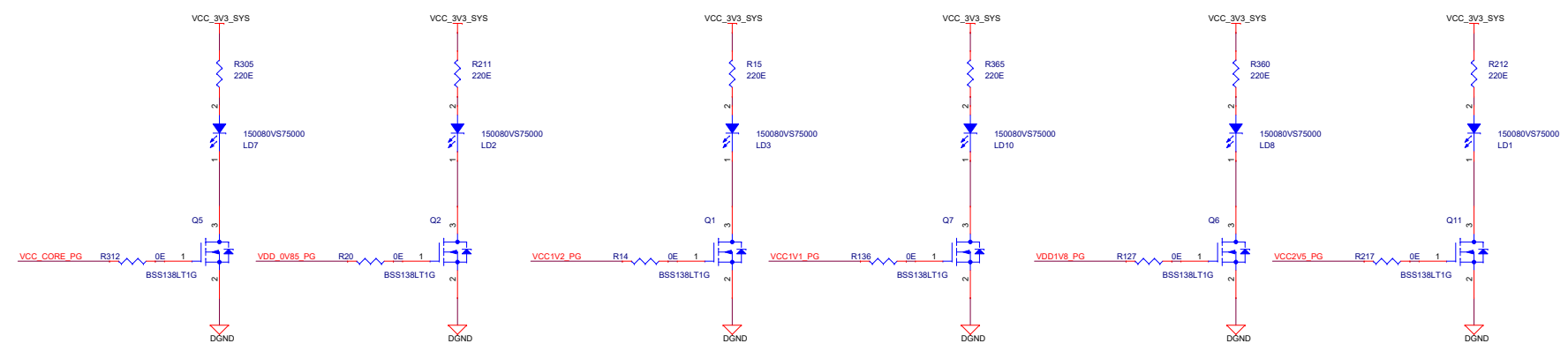
Title DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 35 of 40

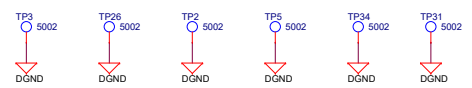
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	38
VDD1V8_PG	VCC1V1_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

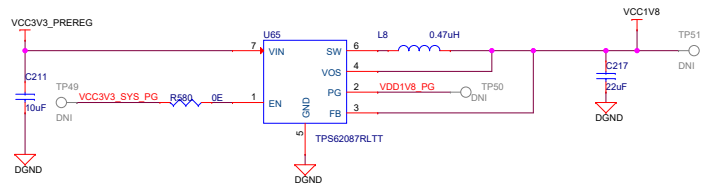
Designed for TI by Mistral Solutions Pvt Ltd



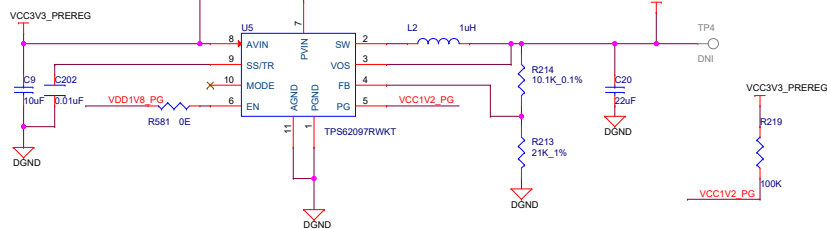
Title MAIN 12V POWERSUPPLY		
Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 36 of 40

SoC POWER SUPPLY

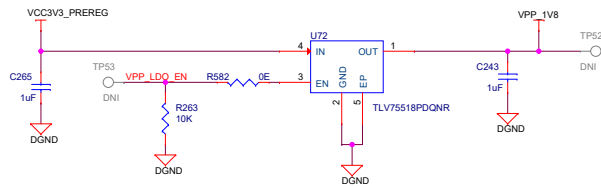
1.8V IO, 3.0AMPS SUPPLY



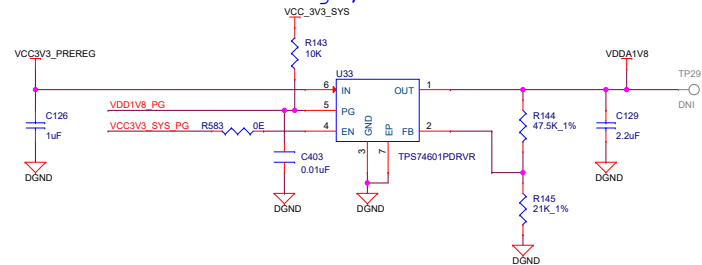
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



1.8V Analog , 1AMPS SUPPLY



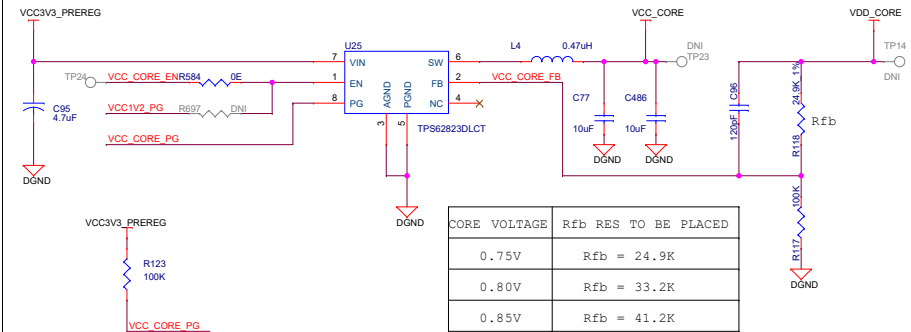
Off Page Connections

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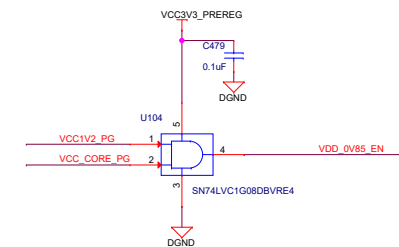
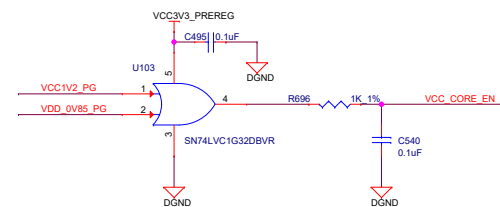
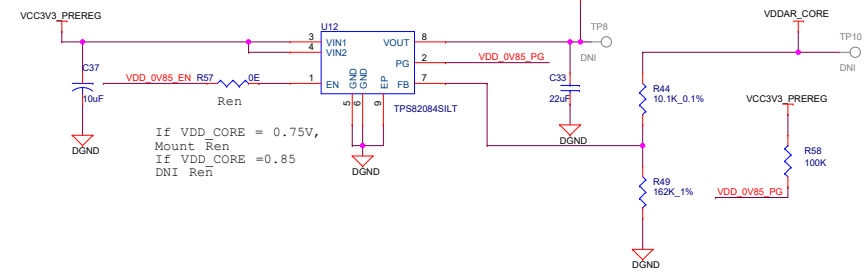
36,37 VCC_CORE_PG  VCC CORE PG
36 VDD_0V85_PG  VDD 0V85 PG
36 VCC1V2_PG    VCC1V2 PG
36 VDD1V8_PG    VDD1V8 PG
33 VPP_LDO_EN    VPP LDO EN
35,37,39 VIN_MON_PORZ_3V3_PG VIN MON PORZ 3V3 PG
37,39 VCC3V3_SYS_PG VCC3V3 SYS PG

```

0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



0.85 V, 1.5AMPS SUPPLY



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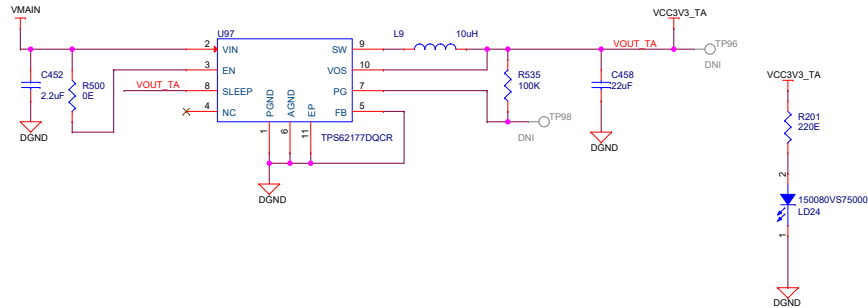


Title	SoC POWER SUPPLY
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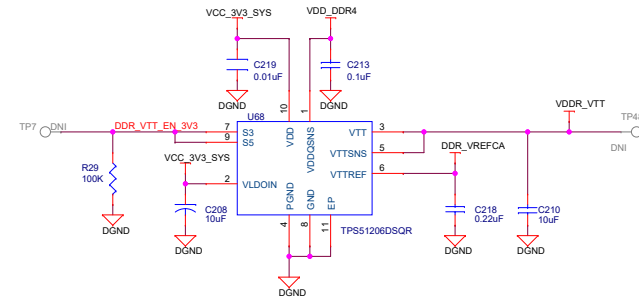
Size	Variant Name = PROC101C(003) TMDS64HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 38 of 40

PERIPHERAL POWER SUPPLY

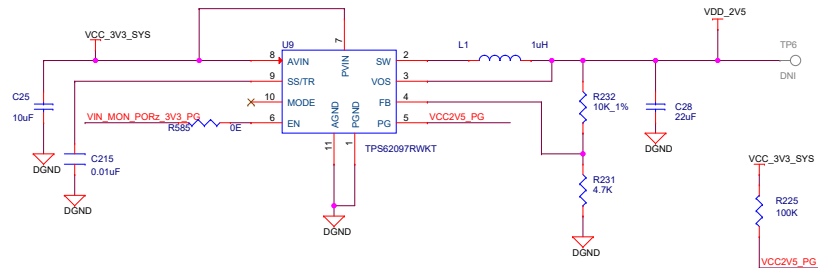
TEST AUTOMATION BOARD POWER



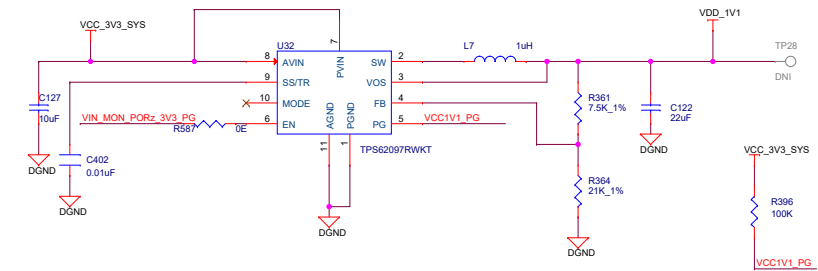
VTT SUPPLY FOR DDR4



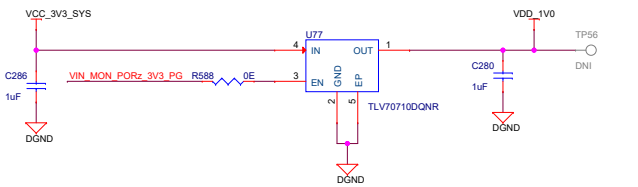
2.5V, 2.0AMPS SUPPLY



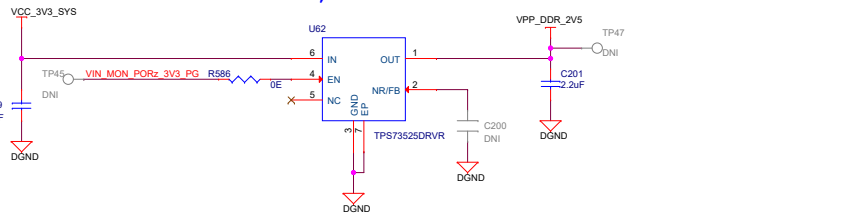
1.1V ETHERNET PHY POWER SUPPLY



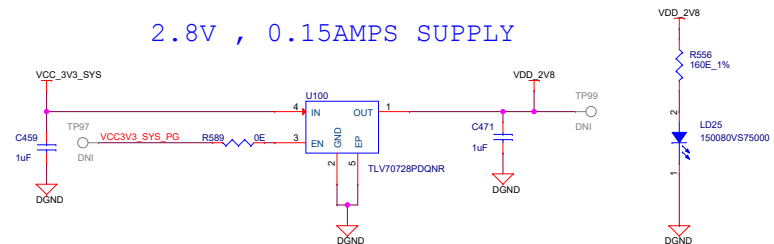
1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY



Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title PERIPHERAL POWER SUPPLY

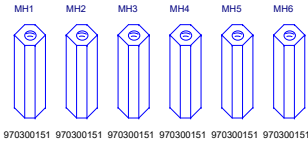
Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 39 of 40

HARDWARE SCHEMATICS

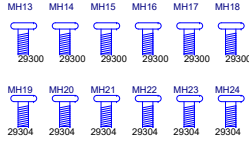
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

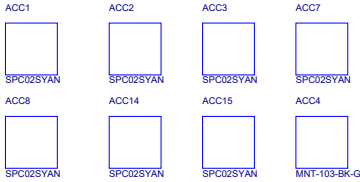
STANDOFFS



SCREWS



JUMPERS



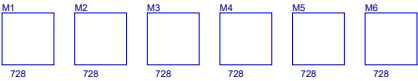
WASHER'S



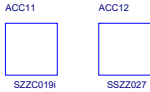
FIDUCIALS



RUBBER FEET



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

Board Serial No.



Assembly Revision

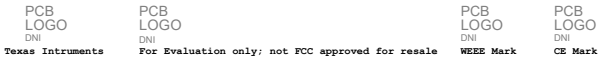


ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOS



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101C(003) TMD564HSEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 40 of 40